

LCFC Confidential

HY568 M/B Schematics Document


Tiger Lake H-Processor with DDR4 + NV GN20-E GPU

2020-10-10

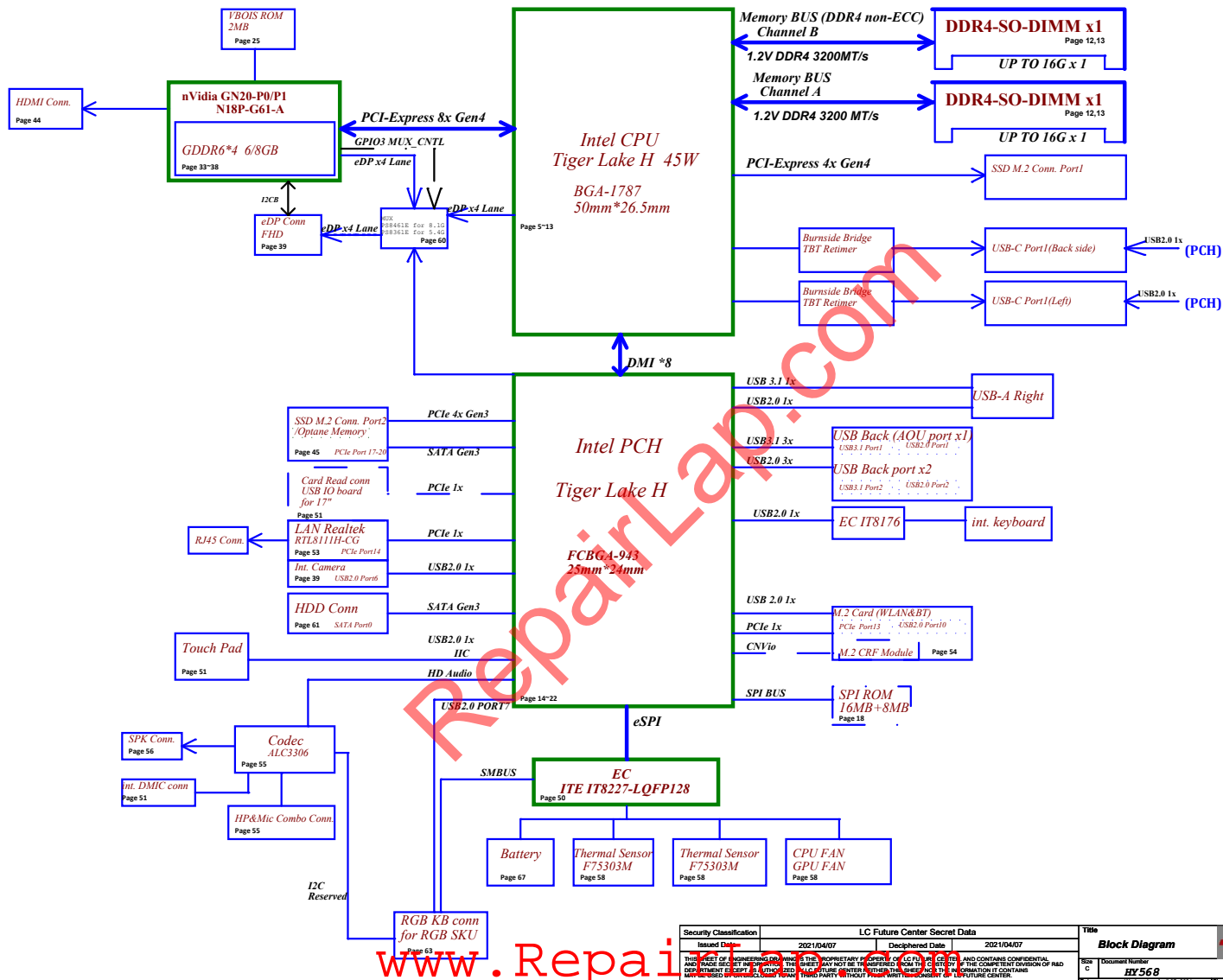
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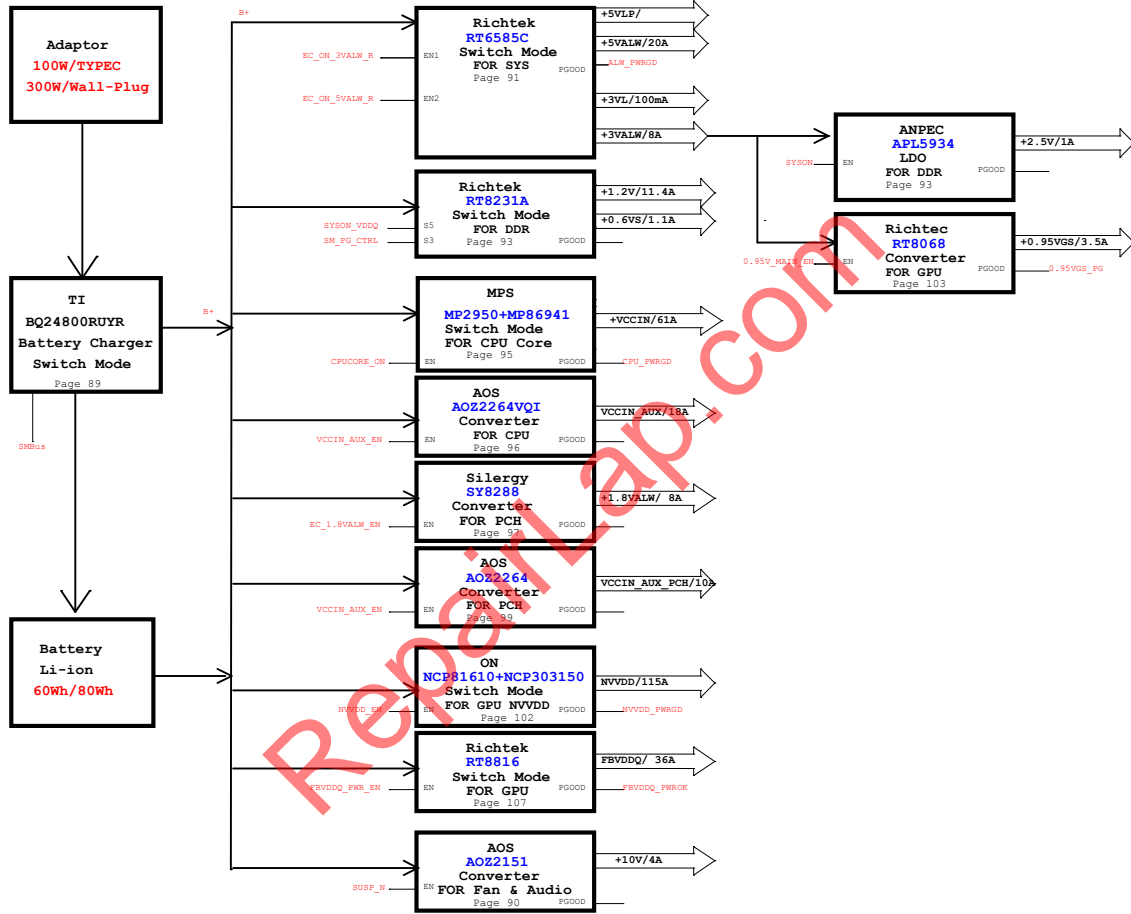
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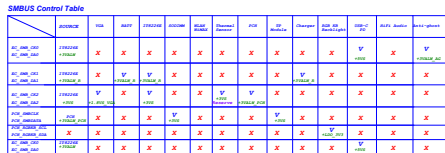
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GN20x-P/N18P-G61-A GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN (10K PD)	
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R (10K PU)	
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL (10K PD)	
GPIO4	OUT	MSVDD_EN 1V8_MAIN_EN	GN20x-P GPU power sequencing for GC6 --MSVDD_EN N18P-G61-A 1V8_MAIN_EN	GPIO4_GC6_MSVDD_EN 1V8_MAIN_EN (10K PU)	
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI (10K PU) RSVD	
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM (100K PD)	
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL (10K PD)	
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT# (10K PU)	
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL (100K PD)	
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_NVDD (10K PD)	
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R (10K PU)	
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	IGPU_EDP_ENBKL (100K PU)	
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD (10K PU)	
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD (10K PU)	
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT (10K PD)	
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD (10K PU)	
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL (100K PD)	
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL (2.2K PU)	
GPIO23	OUT	UNUSED	UNUSED	test point	
GPIO24	IN	HPD_IFPF*	Hot Plug Detect for IFPF	UNUSED	
GPIO25	OUT	FBVDDQ_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI (test point)	
GPIO26	OUT	ROM_WP* FP_FUSE	GN20x-P Connect to WP pin of the GPU EEPROM N18P-G61-A Control FP_FUSE	GPIO26_ROM_WP GPIO26_FP_FUSE (10K PD)	
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD (10K PU)	

H:High: Tied to 1.8V
M:Middle: Tied to 0.9V
L:Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-P/N18P-G61-A VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT51K1256M32JE-14A
L	H	L	2 (0x0002)	Hynix Only For GN20x-P H56CH24AR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVRT# FUNCTION ENABLE

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	N18P-G61-A ENABLE OVERT*
L	L	H	GN20x-P ENABLE OVERT*

BOM NOTE:

1.BOM Structure:
GN20x-P1/P0-->GN20@
N18P-G61-A-->N18P@

2.1.0V GS voltage different: need Power setting
GN20x-P1/P0-->0.95V
N18P-G61-A-->1.0V

3.VBIOS ROM partnumber need BOM control
GN20x-P1/P0-->2MB PN:SA00000AU500
N18P-G61-A-->1MB PN:SA0000080E00

4.ROM SO,ROM SI,ROM_CLK setting
GN20x-P1/P0-->LLH
N18P-G61-A-->LLL

5.VRAM FB(RG702 STUFF package 0402)
GN20x-P1/P0 :2.49K ohm (PN:SD03424918J)
N18P-G61-A: 49.9 ohm (PN:SD034499A8J)

6.+FUSE 1V8
GN20x-P1/P0 :RG1200:10K CG1104:1U
N18P-G61-A: RG1200:2.21K CG1104:2.2U

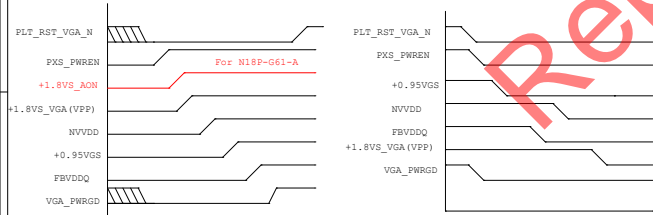
BOM Structure Control Table

BOM Structure	BTO Item
@	Not Support
OPT@	GN20-P1/P0 N18P-G61 Stauf
GN20@	GN20-P1/P0 Stauf
N18P@	N18P-G61 Stauf

STRAP4	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

GN20x-P/N18P-G61-A Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 20us.
2. It is recommended that the delay from 1V8 on to FBVDDQ/GPU_P0000 assertion not exceed 20us.
3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVVDD must be 90s before FBVDDQ can ramp-up.
5. Refer to the JEDEC Memory SPEC for memory-related power sequencing.
7. FBVDDQ, USB_VDDP and 1V8_AON don't need power cycle for GC6

1. For GC6B6, VSP must be equal to or higher than FBVDDQ at all times; use gate logic and discharge circuit as needed.
2. All 3.3V devices that connect to the GPU must be ramp down before 1V8. GPU can NOT have any 3.3V leakage path after 1V8 power down.
3. Power down of FBVDDQ must be less than 10s before NVVDD can start ramp-down.

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	N18E VGA Notes List	Rev. 568
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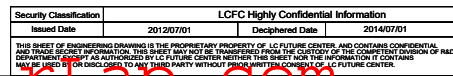
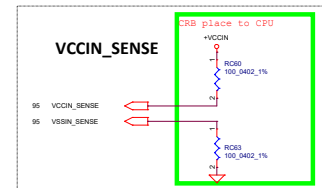
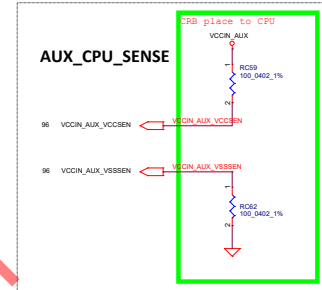
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		CPU (1/9) DMI, PEG							



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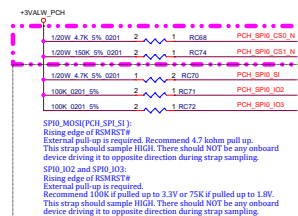
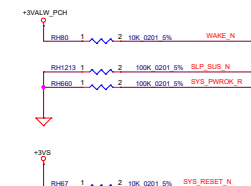
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Size	Document Number				
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1	UCIN	4.3A	1.2V
115	VSS 572 V002	1	BM15
116	VSS 573 V002	2	BM16
117	VSS 574 V002	3	AJ11
118	VSS 575 V002	4	AL11
119	VSS 576 V002	5	AM11
120	VSS 577 V002	6	AM12
121	VSS 578 V002	7	AM13
122	VSS 579 V002	8	AM14
123	VSS 580 V002	9	AM15
124	VSS 581 V002	10	AM16
125	VSS 582 V002	11	AM17
126	VSS 583 V002	12	AM18
127	VSS 584 V002	13	AM19
128	VSS 585 V002	14	AM20
129	VSS 586 V002	15	AM21
130	VSS 587 V002	16	AM22
131	VSS 588 V002	17	AM23
132	VSS 589 V002	18	AM24
133	VSS 590 V002	19	AM25
134	VSS 591 V002	20	AM26
135	VSS 592 V002	21	AM27
136	VSS 593 V002	22	AM28
137	VSS 594 V002	23	AM29
138	VSS 595 V002	24	AM30
139	VSS 596 V002	25	AM31
140	VSS 597 V002	26	AM32
141	VSS 598 V002	27	AM33
142	VSS 599 V002	28	AM34
143	VSS 600 V002	29	AM35
144	VSS 601 V002	30	AM36
145	VSS 602 V002	31	AM37
146	VSS 603 V002	32	AM38
147	VSS 604 V002	33	AM39
148	VSS 605 V002	34	AM40
149	VSS 606 V002	35	AM41
150	VSS 607 V002	36	AM42
151	VSS 608 V002	37	AM43
152	VSS 609 V002	38	AM44
153	VSS 610 V002	39	AM45
154	VSS 611 V002	40	AM46
155	VSS 612 V002	41	AM47
156	VSS 613 V002	42	AM48
157	VSS 614 V002	43	AM49
158	VSS 615 V002	44	AM50
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162	VSS 619 V002	48	AM54
163	VSS 620 V002	49	AM55
164	VSS 621 V002	50	AM56
165	VSS 622 V002	51	AM57
166	VSS 623 V002	52	AM58
167	VSS 624 V002	53	AM59
168	VSS 625 V002	54	AM60
169	VSS 626 V002	55	AM61
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171	VSS 628 V002	57	AM63
172	VSS 629 V002	58	AM64
173	VSS 630 V002	59	AM65
174	VSS 631 V002	60	AM66
175	VSS 632 V002	61	AM67
176	VSS 633 V002	62	AM68
177	VSS 634 V002	63	AM69
178	VSS 635 V002	64	AM70
179	VSS 636 V002	65	AM71
180	VSS 637 V002	66	AM72
181	VSS 638 V002	67	AM73
182	VSS 639 V002	68	AM74
183	VSS 640 V002	69	AM75
184	VSS 641 V002	70	AM76
185	VSS 642 V002	71	AM77
186	VSS 643 V002	72	AM78
187	VSS 644 V002	73	AM79
188	VSS 645 V002	74	AM80
189	VSS 646 V002	75	AM81
190	VSS 647 V002	76	AM82
191	VSS 648 V002	77	AM83
192	VSS 649 V002	78	AM84
193	VSS 650 V002	79	AM85
194	VSS 651 V002	80	AM86

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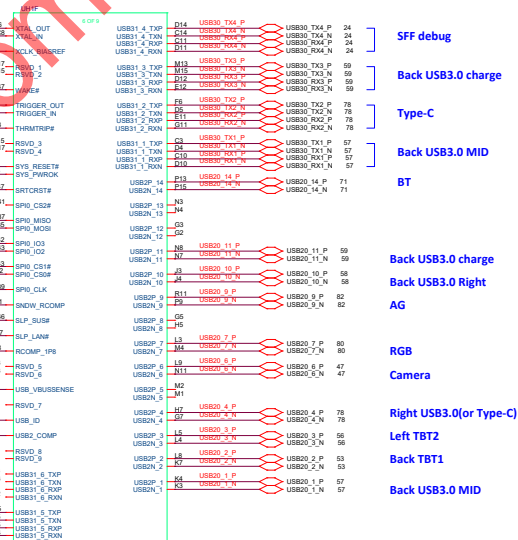
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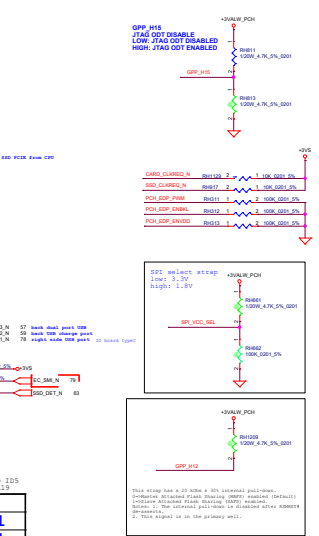
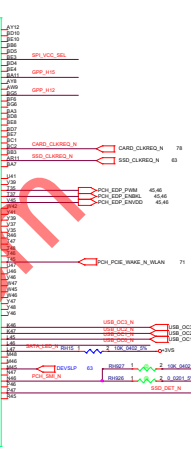
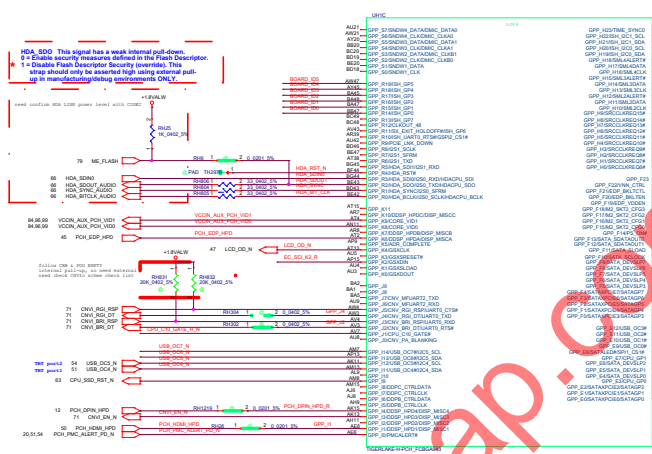
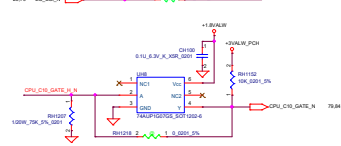
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C		PCH (2/8) USB, SPI							



Function	BOARD ID0	BOARD ID1	BOARD ID2	BOARD ID3	BOARD ID4	BOARD ID5
	GPF_R14	GPF_R15	GPF_R16	GPF_R17	GPF_R18	GPF_R19
	SRU Size			GPU Type		
HY568-15-GN20E-E3	0	0	1	0	0	1
HY568-17-GN20E-E3	0	1	0	0	0	1
HY568-15-GN20E-E	0	0	1	0	1	0
E5 HY568P-GN20E-E	0	1	1	0	0	1
HY568P-GN20E-E5	0	1	1	0	1	0
Y760-GN20E-E3	1	0	0	0	0	1
Y760-GN20E-E5	1	0	0	0	1	0
Y760-GN20E-E7	1	0	0	0	1	1
HY568-15-GN20P-P0	0	0	1	1	0	0
HY568-17-GN20P-P0	0	1	0	1	0	0
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HY568-17-GN20P-P1	0	1	0	1	0	1
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HY568-17-N18P-G61	0	1	0	1	1	0
HY568-15-GN20P0-P0	0	0	1	1	1	1

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LH14		
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A1Z	VSS 16WVS 240	A1Z2
A2	VSS 16WVS 241	A22
A3	VSS 16WVS 242	A32
A4	VSS 16WVS 243	A42
A5	VSS 16WVS 244	A52
A6	VSS 16WVS 245	A62
A7	VSS 16WVS 246	A72
A8	VSS 16WVS 247	A82
A9	VSS 16WVS 248	A92
A10	VSS 16WVS 249	A102
A11	VSS 16WVS 250	A112
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A19	VSS 16WVS 258	A192
A20	VSS 16WVS 259	A202
A21	VSS 16WVS 260	A212
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A56	VSS 16WVS 295	A562
A57	VSS 16WVS 296	A572
A58	VSS 16WVS 297	A582
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A73	VSS 16WVS 312	A732
A74	VSS 16WVS 313	A742
A75	VSS 16WVS 314	A752
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LH15		
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A7	VSS 16WVS 246	A72
A8	VSS 16WVS 247	A82
A9	VSS 16WVS 248	A92
A10	VSS 16WVS 249	A102
A11	VSS 16WVS 250	A112
A12	VSS 16WVS 251	A122
A13	VSS 16WVS 252	A132
A14	VSS 16WVS 253	A142
A15	VSS 16WVS 254	A152
A16	VSS 16WVS 255	A162
A17	VSS 16WVS 256	A172
A18	VSS 16WVS 257	A182
A19	VSS 16WVS 258	A192
A20	VSS 16WVS 259	A202
A21	VSS 16WVS 260	A212
A22	VSS 16WVS 261	A222
A23	VSS 16WVS 262	A232
A24	VSS 16WVS 263	A242
A25	VSS 16WVS 264	A252
A26	VSS 16WVS 265	A262
A27	VSS 16WVS 266	A272
A28	VSS 16WVS 267	A282
A29	VSS 16WVS 268	A292
A30	VSS 16WVS 269	A302
A31	VSS 16WVS 270	A312
A32	VSS 16WVS 271	A322
A33	VSS 16WVS 272	A332
A34	VSS 16WVS 273	A342
A35	VSS 16WVS 274	A352
A36	VSS 16WVS 275	A362
A37	VSS 16WVS 276	A372
A38	VSS 16WVS 277	A382
A39	VSS 16WVS 278	A392
A40	VSS 16WVS 279	A402
A41	VSS 16WVS 280	A412
A42	VSS 16WVS 281	A422
A43	VSS 16WVS 282	A432
A44	VSS 16WVS 283	A442
A45	VSS 16WVS 284	A452
A46	VSS 16WVS 285	A462
A47	VSS 16WVS 286	A472
A48	VSS 16WVS 287	A482
A49	VSS 16WVS 288	A492
A50	VSS 16WVS 289	A502
A51	VSS 16WVS 290	A512
A52	VSS 16WVS 291	A522
A53	VSS 16WVS 292	A532
A54	VSS 16WVS 293	A542
A55	VSS 16WVS 294	A552
A56	VSS 16WVS 295	A562
A57	VSS 16WVS 296	A572
A58	VSS 16WVS 297	A582
A59	VSS 16WVS 298	A592
A60	VSS 16WVS 299	A602
A61	VSS 16WVS 300	A612
A62	VSS 16WVS 301	A622
A63	VSS 16WVS 302	A632
A64	VSS 16WVS 303	A642
A65	VSS 16WVS 304	A652
A66	VSS 16WVS 305	A662
A67	VSS 16WVS 306	A672
A68	VSS 16WVS 307	A682
A69	VSS 16WVS 308	A692
A70	VSS 16WVS 309	A702
A71	VSS 16WVS 310	A712
A72	VSS 16WVS 311	A722
A73	VSS 16WVS 312	A732
A74	VSS 16WVS 313	A742
A75	VSS 16WVS 314	A752
A76	VSS 16WVS 315	A762
A77	VSS 16WVS 316	A772
A78	VSS 16WVS 317	A782
A79	VSS 16WVS 318	A792
A80	VSS 16WVS 319	A802


TIGERLAKE-H-PCH_FCB0643

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R587	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

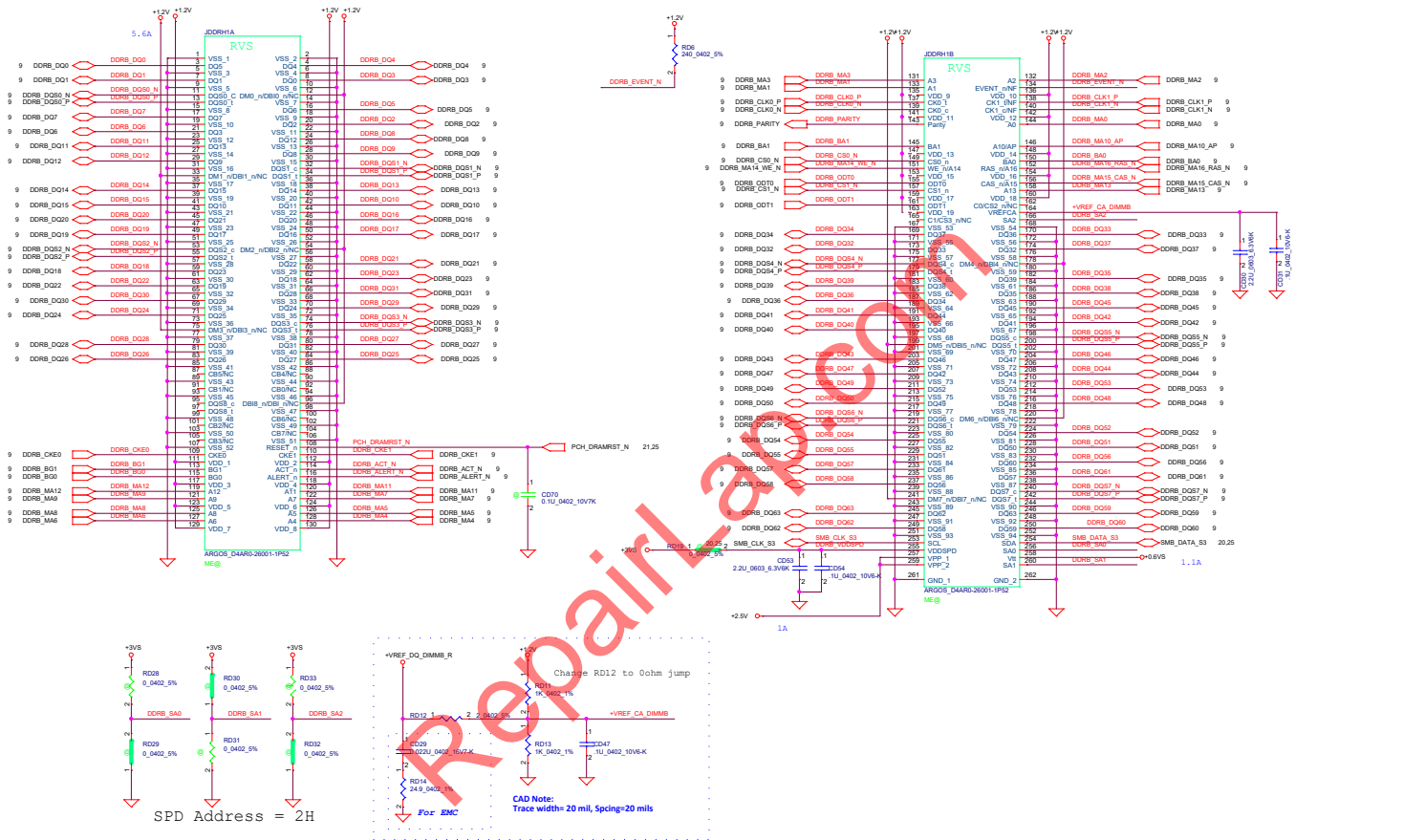



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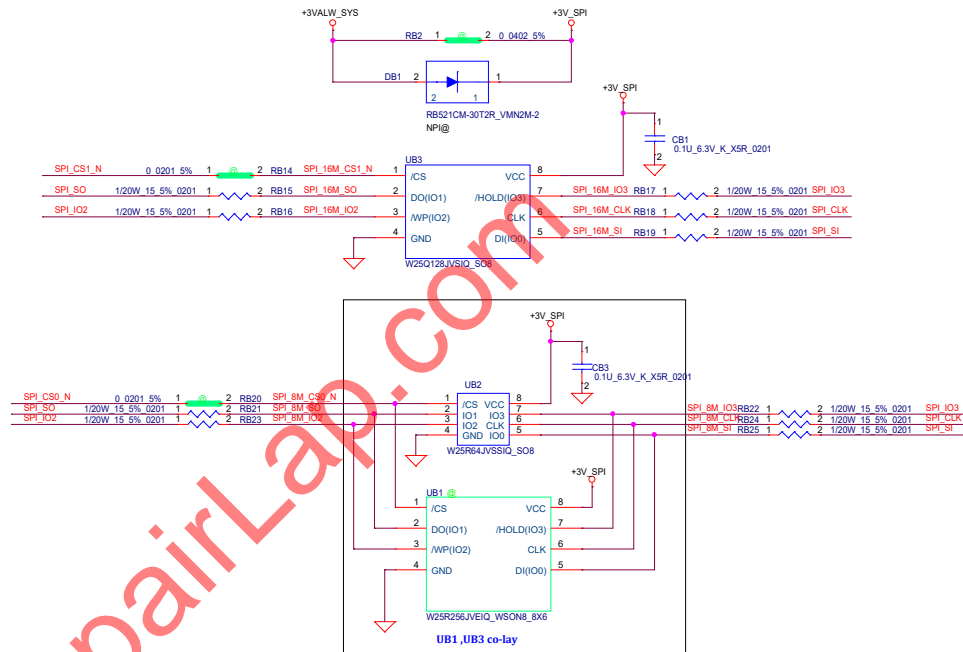
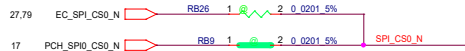
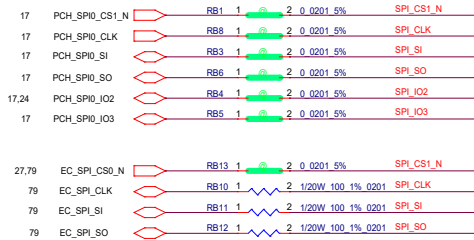
The schematic shows a circuit for the DDRA_EVENT_N pin. A red line representing the signal trace enters from the bottom left and connects to the pin. A resistor, labeled RD5 with a value of 240_0402_5%, is connected between the pin and a 1.2V supply. The 1.2V supply is indicated by a red circle with a red line extending upwards, labeled "CR2 Gohm_0403 to 1.2V+1.2V".



DDR4 SO-DIMM B
Follow CRB ball map TOP 5.2 Height

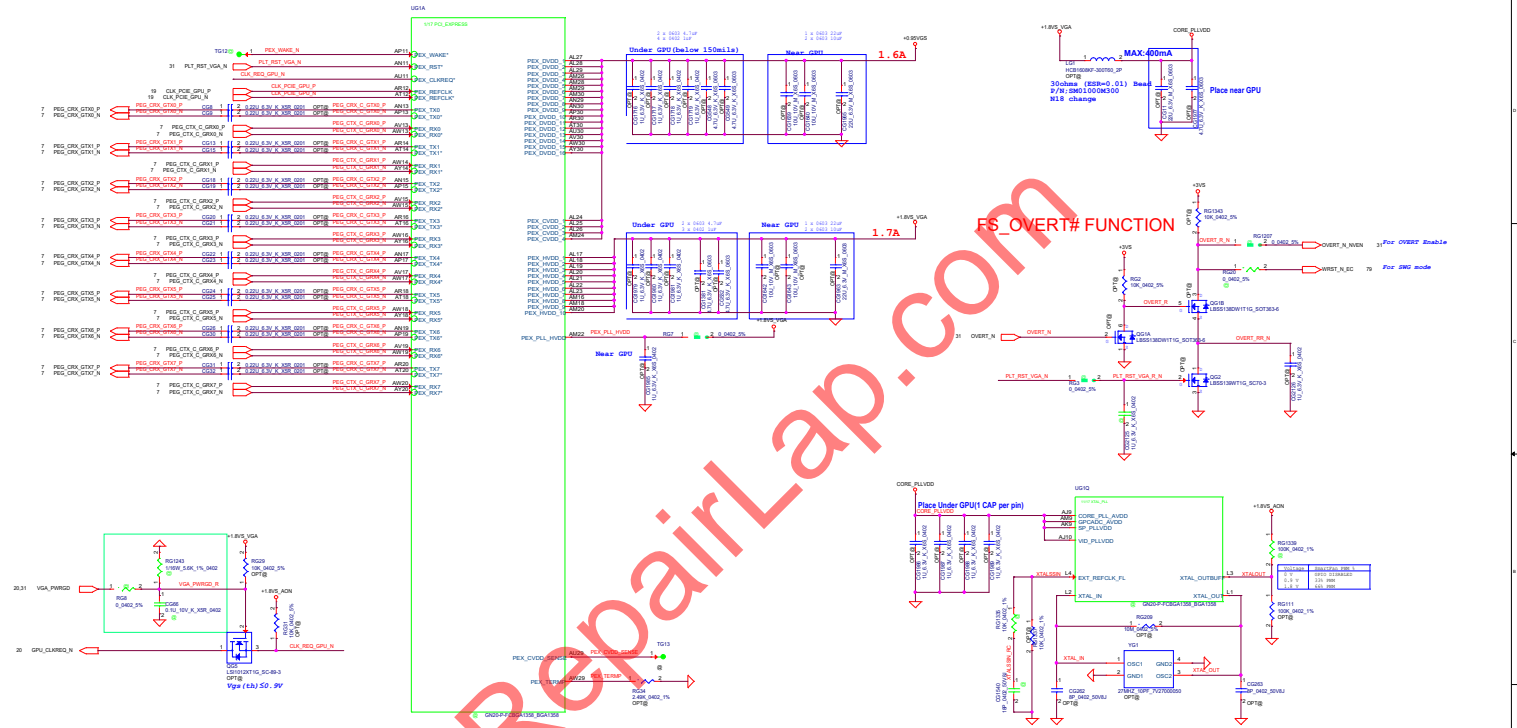


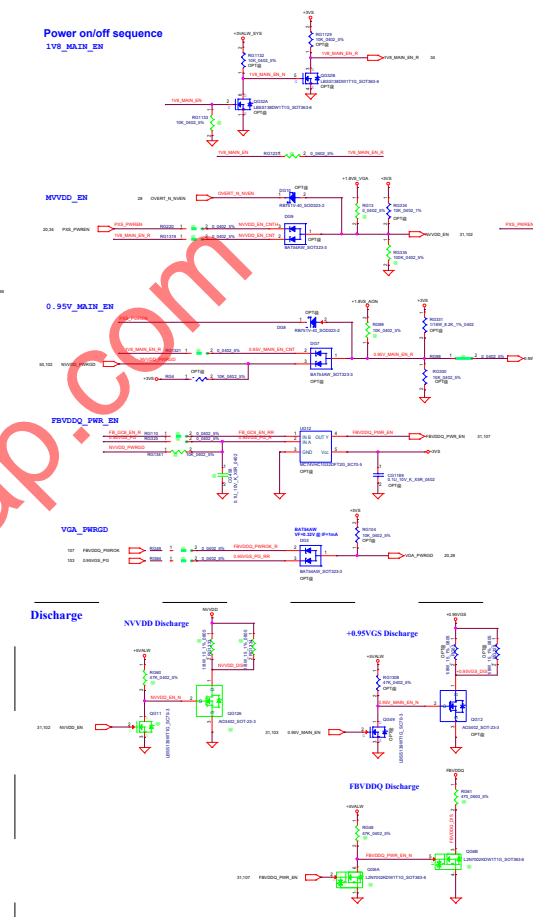
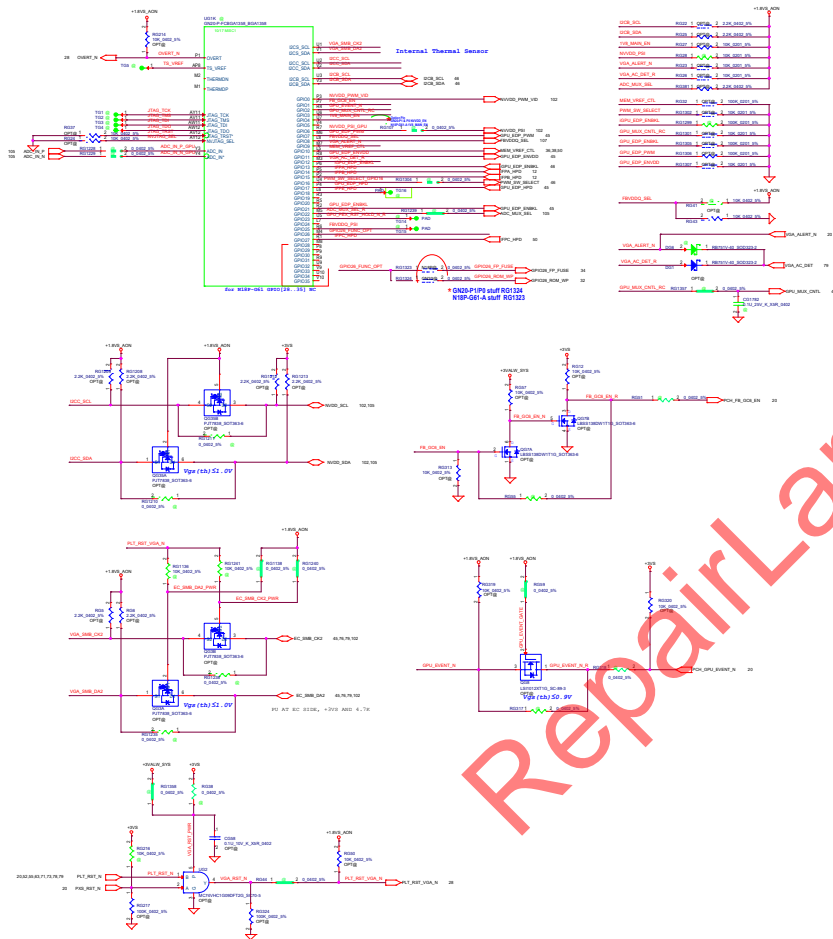
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Issued Date	2021/04/07	Deciphered Date	2021/04/07	DDRVI SO-DIMM B	
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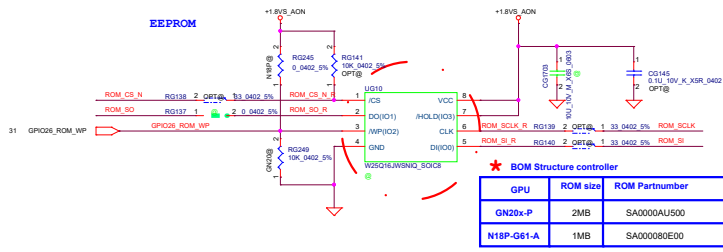
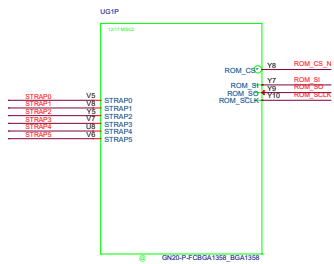


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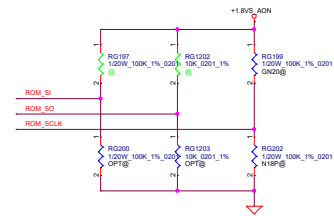






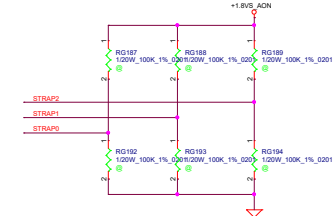
★ BOM Structure controller

GPU	ROM size	ROM Partnumber
GN20x-P	2MB	SA0000AU500
N18P-G61-A	1MB	SA0000B0E00



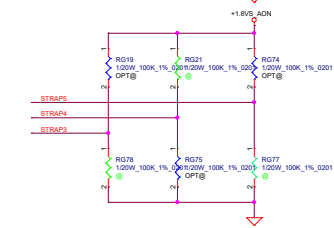
1:ENABLE 0:DISABLE
SOR1/2/3 ENABLE

GPU	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N18P-G61-A	L	L	L	ENABLE OVERT*
GN20x-P	L	L	H	ENABLE OVERT*



VRAMCFG

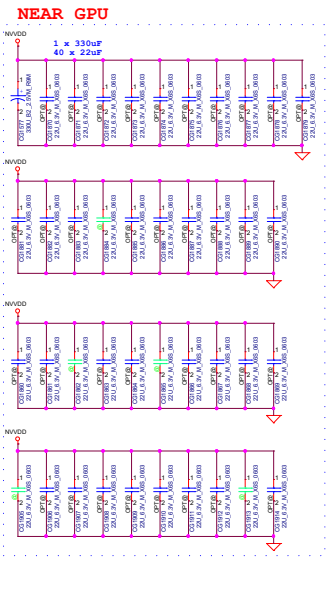
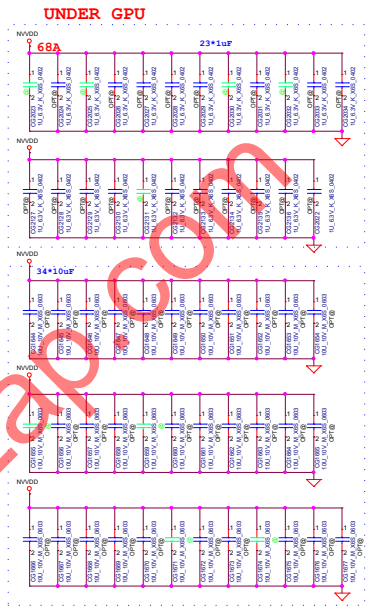
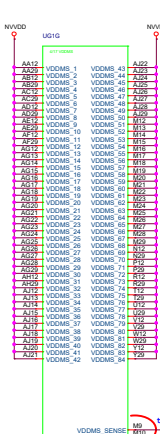
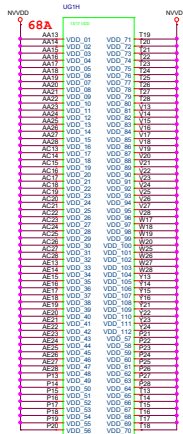
GPU VRAM	FB Memory (GDDR6)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
GN20x-P1	Samsung 8Gb	K4E803258C-NC14	0 (0x0000)	L	L	L
GN20x-P0	Micron 8Gb	MT61K256M32JE-14	1 (0x0001)	L	L	H
N18P-G61-A 4GB	Hynix 8Gb	H56CBH24NR-82C	2 (0x0002)	L	H	L



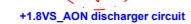
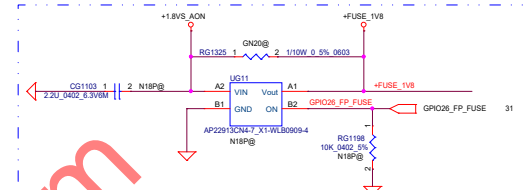
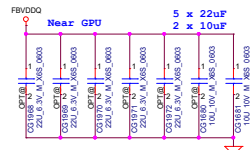
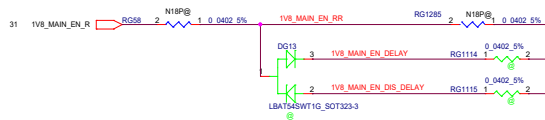
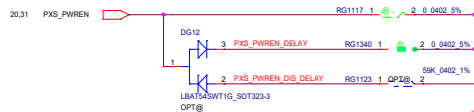
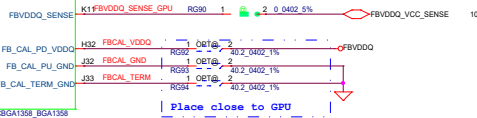
VGA_DEVICE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

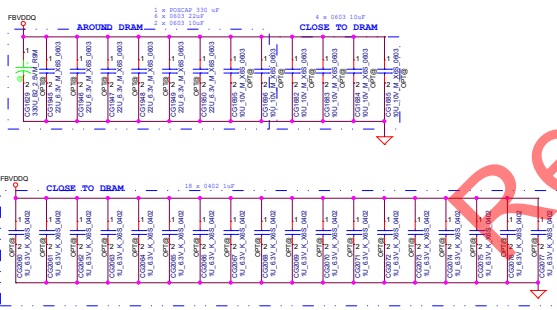
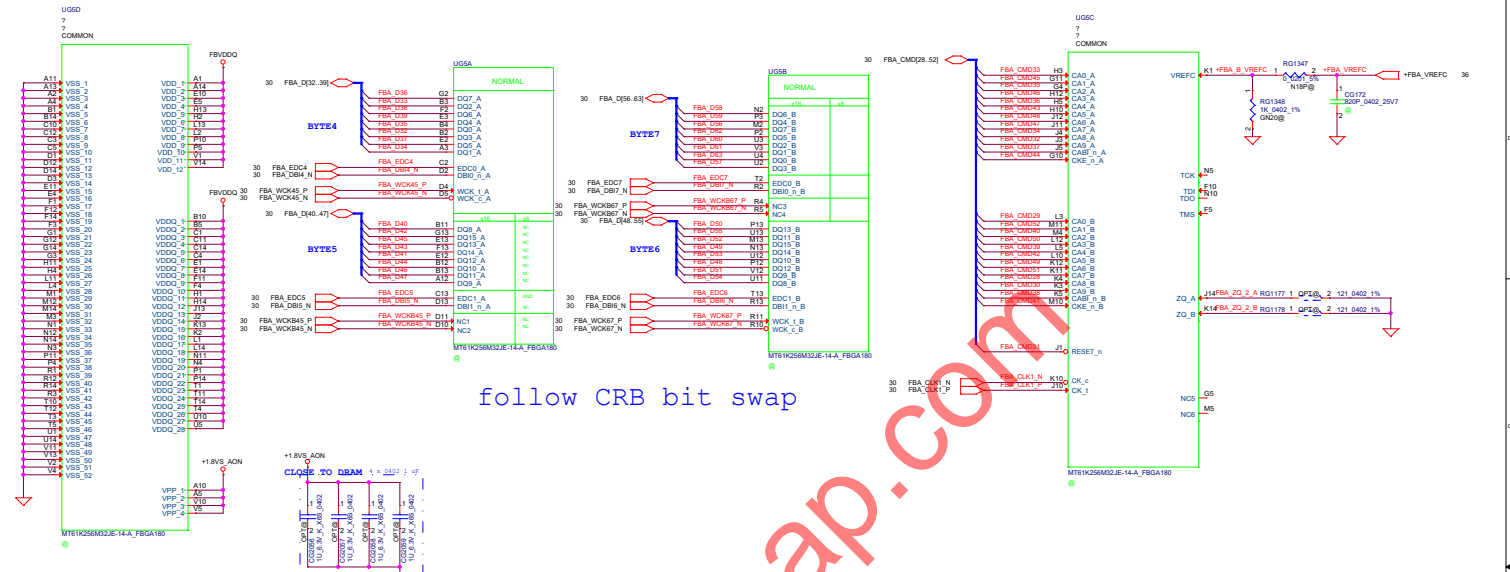
- 1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE
- 1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGINAL
- 1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER
- 1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE
- 1: DEVID_SEL for G-SYNC SKU

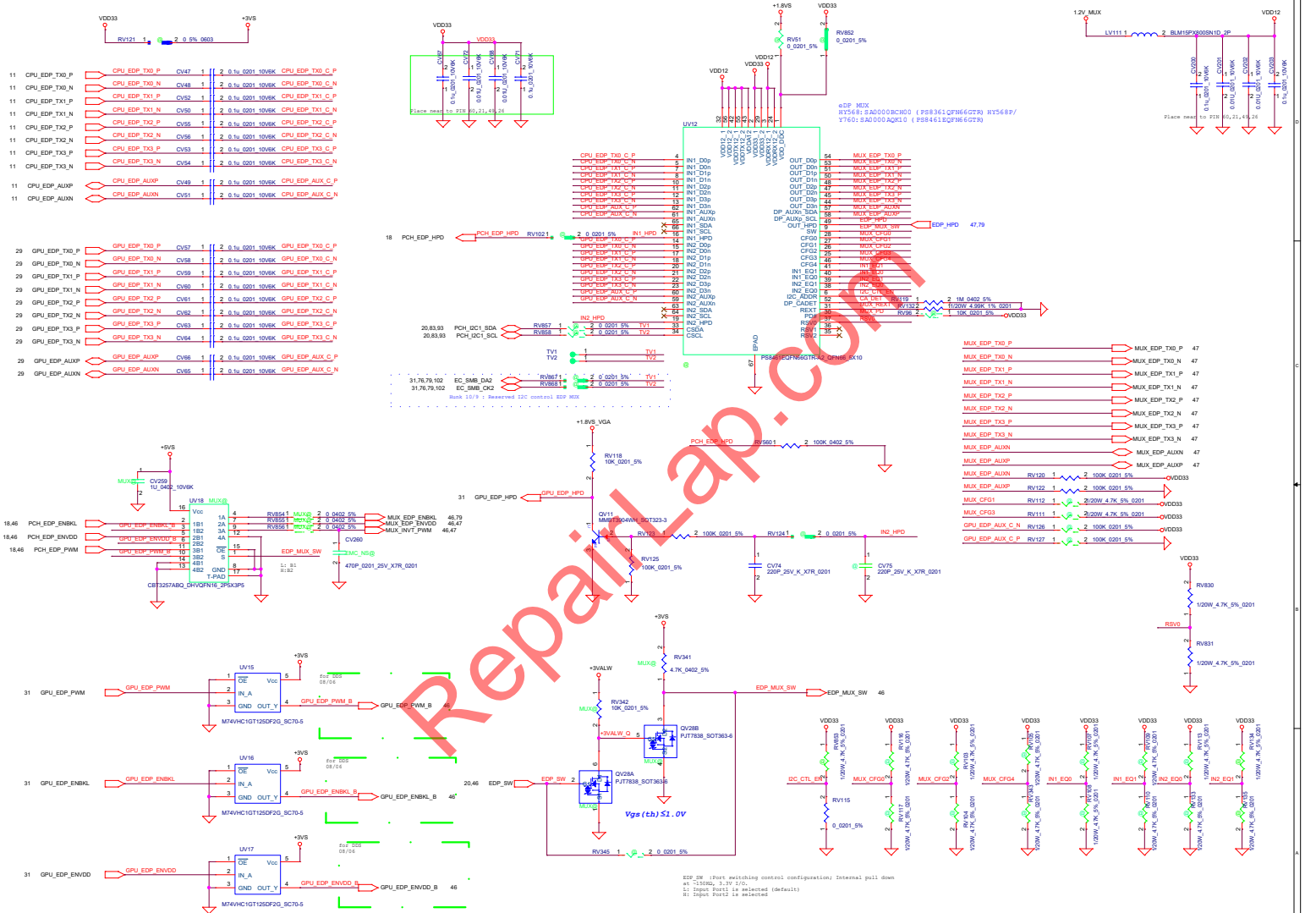


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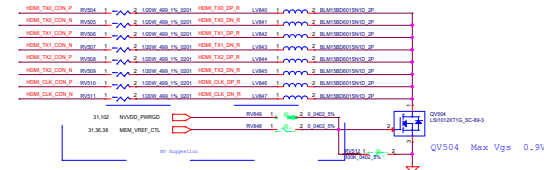
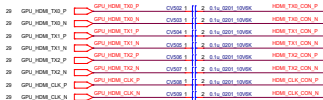
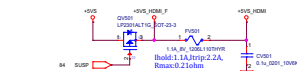


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Doc Number	HY568				Rev
Doc	Wednesday, April 07, 2021				45 of 118

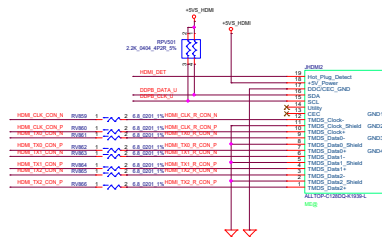
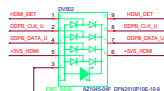
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Size	Document Number		Rev	
Quantity	HY568		1.0	
Drawing No. HY- 021			Issue	of

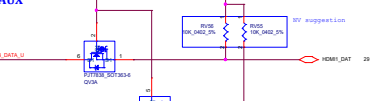
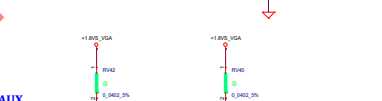
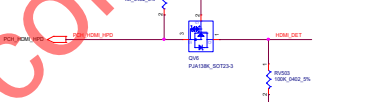
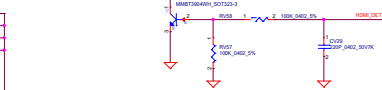
HDMI Power



EMC



update by bing
20180316



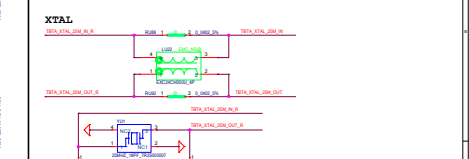
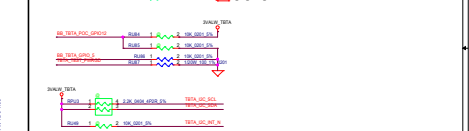
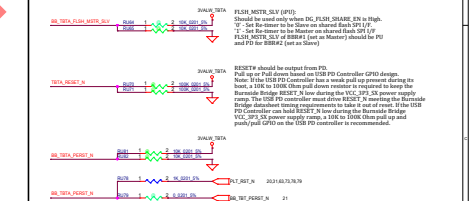
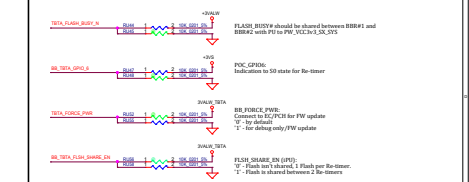
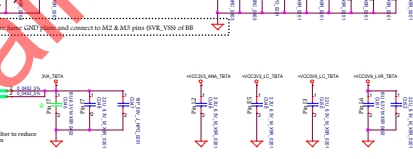
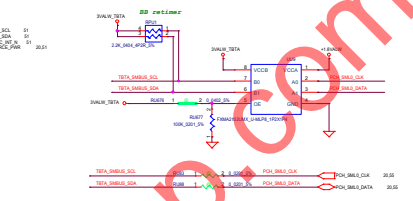
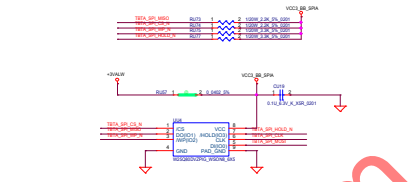
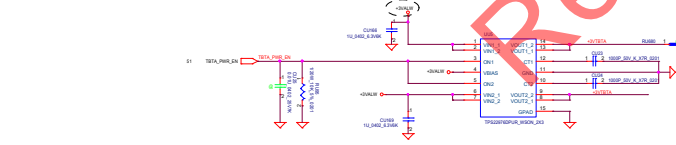
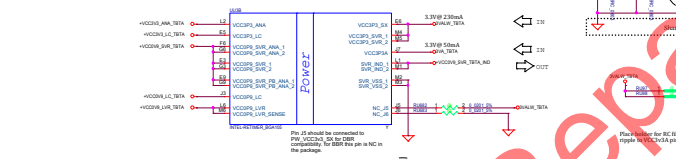
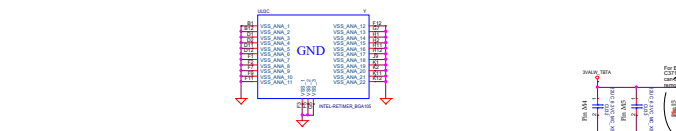
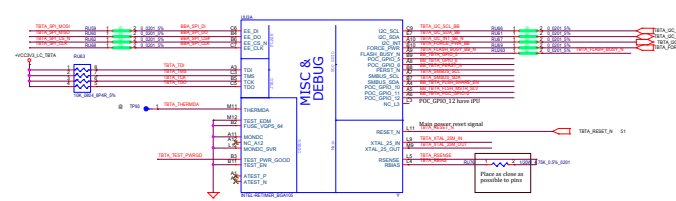
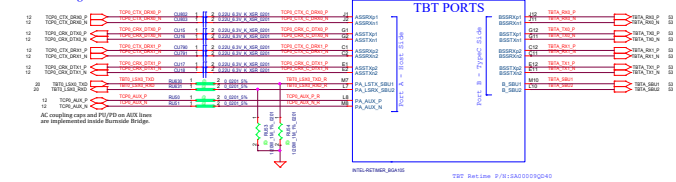
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Revised Date	20180702	Disciplined Date	20180704
HDMI_CONN			LCFC
Revised By			RY568
Revised Date			20180704



I2C1	Master: EC	TBTB PORT	0x23
	Slave: FD	TBTC PORT	0x27
I2C2	Master: PMC	TBTB PORT	0x23
	Slave: FD	TBTC PORT	0x27
I2C3	Master: FD	TBTB PORT	T.B.D.
	Slave: RT	TBTC PORT	T.B.D.

[illegible]

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TBT portB/left side

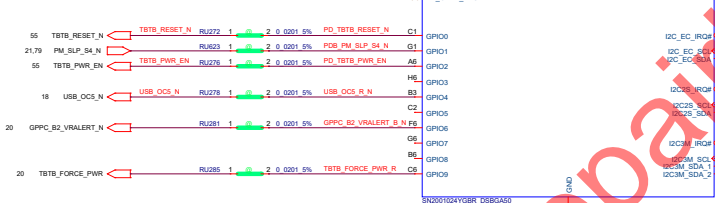
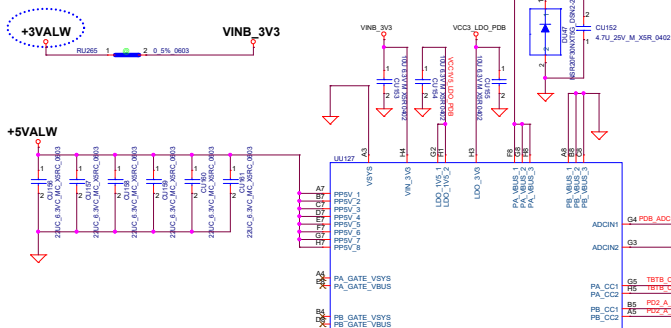
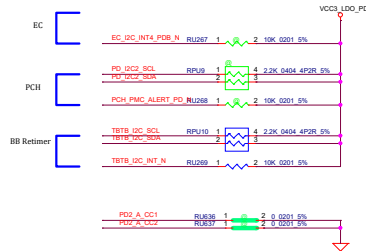
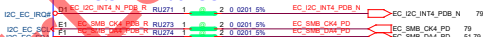


TABLE I2C Addressing

ADCIN1:3 ADCIN2:0	I2C1	Master: EC	TBTB PORT	0x23
		Slave: PD	TBTC PORT	0x22
	I2C2	Master: PMC	TBTB PORT	0x23
		Slave: PD	TBTC PORT	0x22
	I2C3	Master: PD	TBTB PORT	T.B.D.
		Slave: RT	TBTC PORT	T.B.D.



PH 3.3VALW at EC SIDE



PH 3.3 VALW at PCH SIDE



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TYPEC Controller PortA

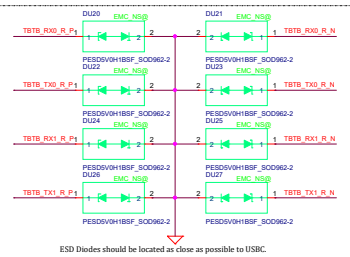
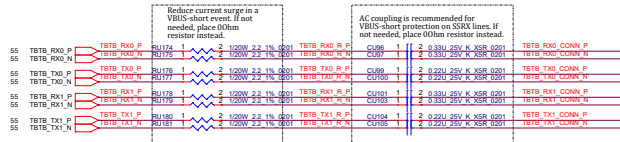
Rev

Date: Wednesday, April 07, 2021 Sheet 64 of 11

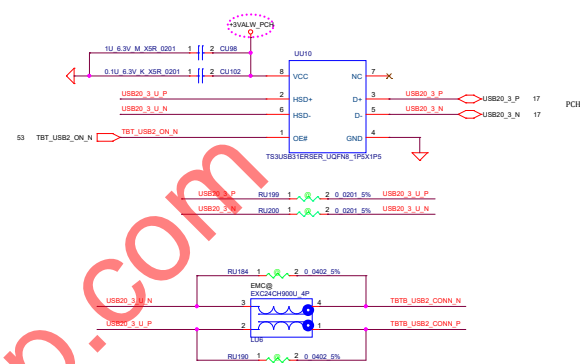
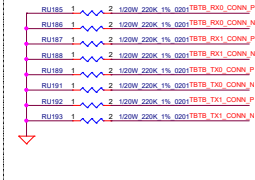
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1110

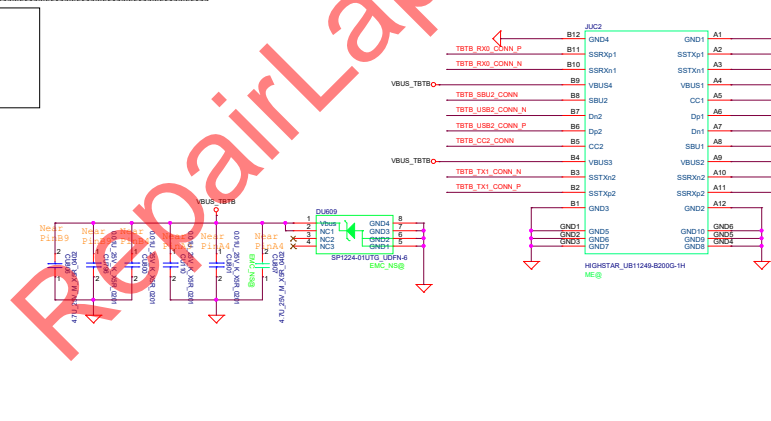
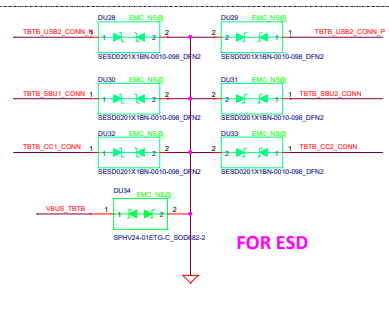
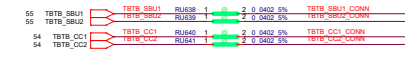




Bleeding SSTX/SRRX resistors must be placed near USBC connector if 330nF cap is being used. Otherwise de-populate.

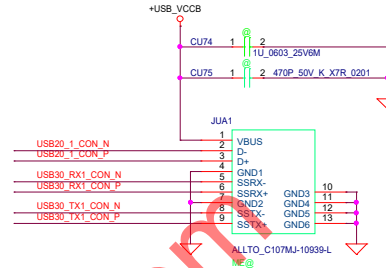
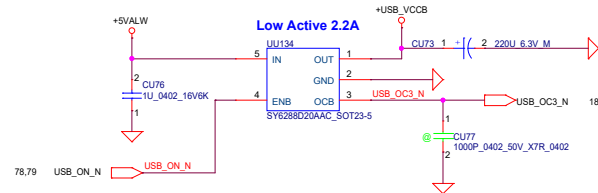


Remove CC OVP

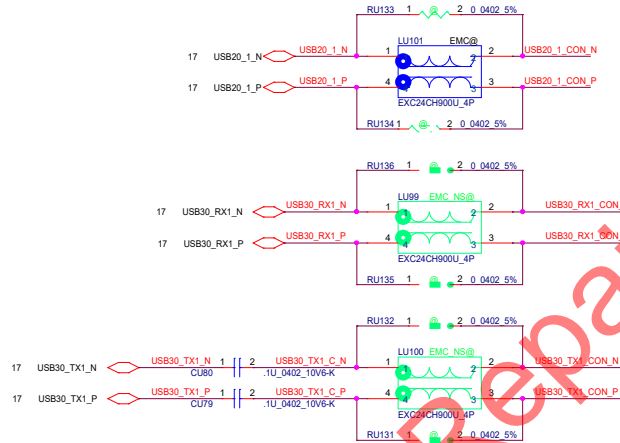
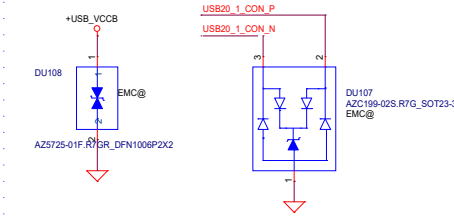
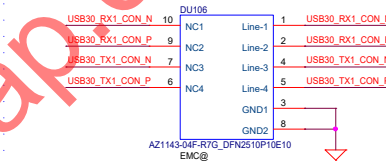


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Date		Wednesday, April 07, 2011		Printed	
Page		56		of 110	

USB1.1 PORT x2

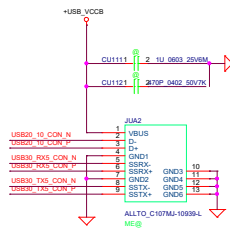


EMC close to USB Conn

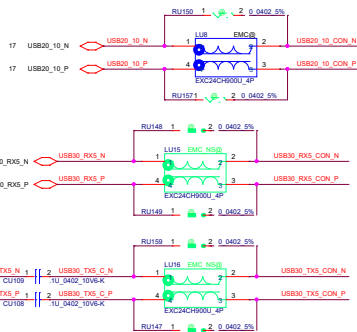
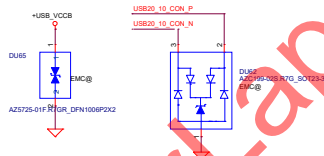


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Title	USB2.0
Size	Document Number
Rev	0.1
Date	Wednesday, April 07, 2021
Sheet	57 of 110

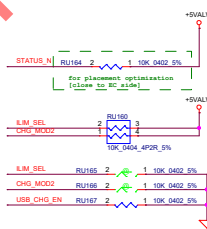
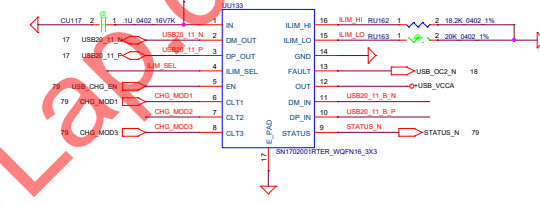
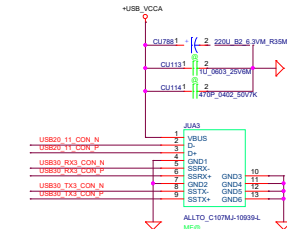
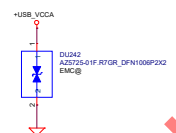
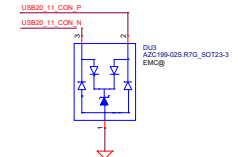
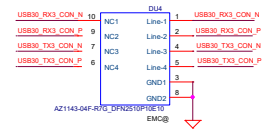
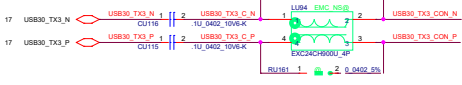
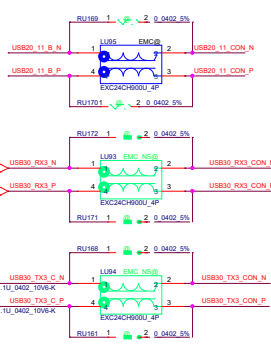


EMC close to USB Conn



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Issued Date		Deciphered Date		USB2.0	
2021/04/07		2021/04/07		Rev	
Size		Document Number		HY568	
C		0.1		Date	
Wednesday, April 07, 2021		Sheet		36 of 119	

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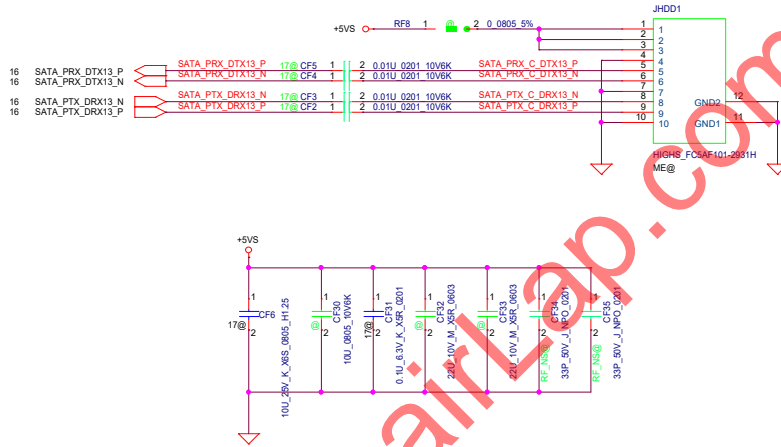
USB charger
2.5A

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0	0	0	X	DCR
1	1	1	1	CDP
1	1	1	0	SDP2
1	1	0	X	SDP1
0	1	0	X	SDP1
1	0	0	X	DCP_Boast
1	0	1	X	DCP_Divider
0	1	1	X	DCP_Auto
0	0	1	X	DCP_Auto

Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		USB2.0/USB3.0 PORT (LEFT)	
2021/04/07		2021/04/07		Size C	
2021/04/07		2021/04/07		Document Number	
2021/04/07		2021/04/07		BY 568	
2021/04/07		2021/04/07		Date	
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2021/04/07		2021/04/07		Sheet 39 of 119	

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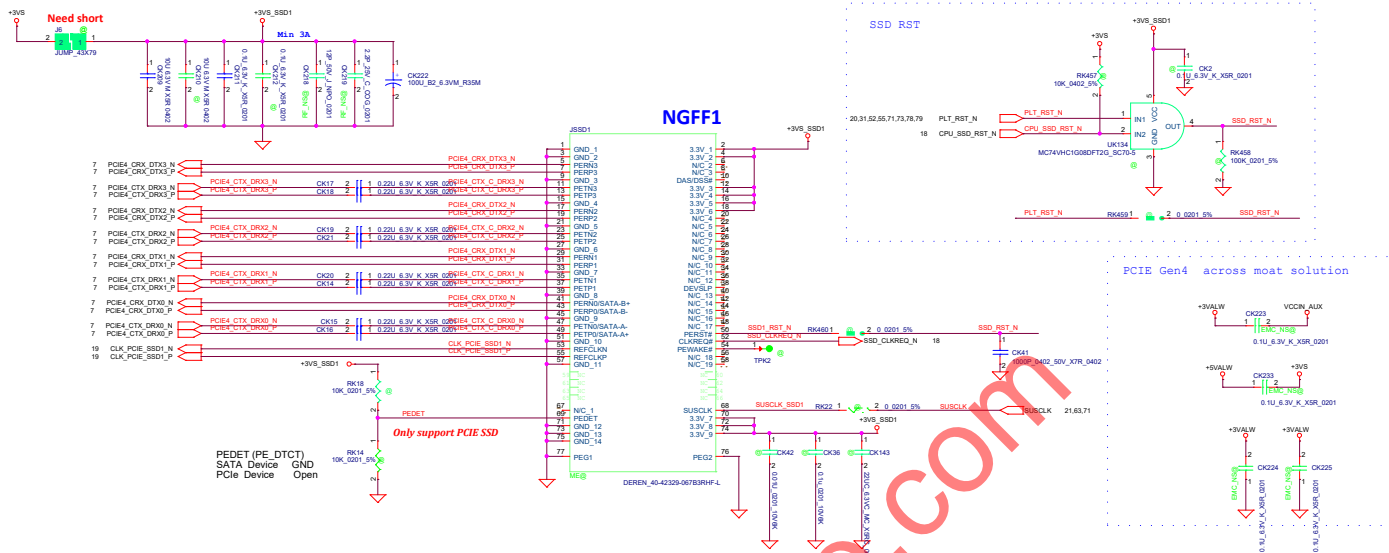
SATA HDD Conn.



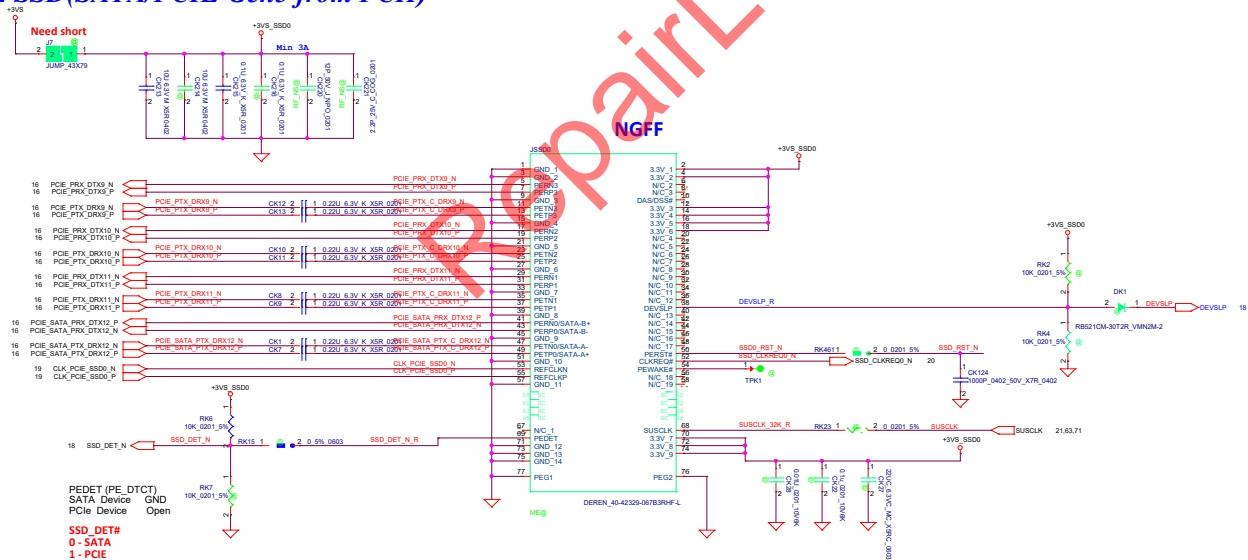
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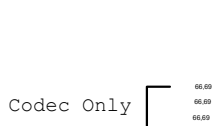
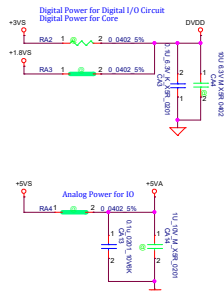
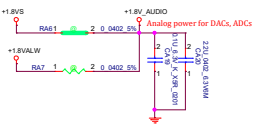
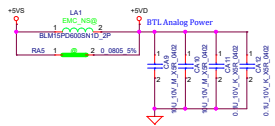
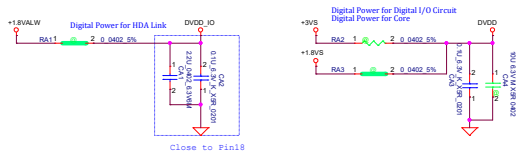
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HDD/XBOX CONN			
Size	Document Number	Rev	
B	HY568	0.3	
Date:	Wednesday, April 07, 2021	Sheet	61 of 110

M.2 SSD(PCIE GEN4 from CPU)

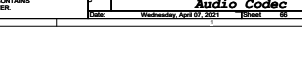
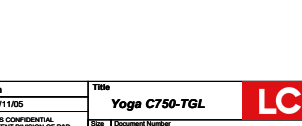
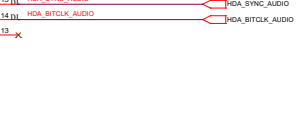
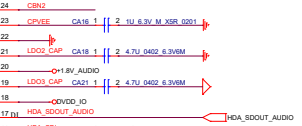
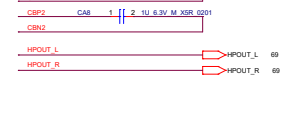
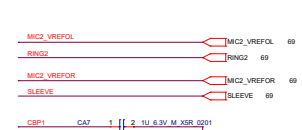
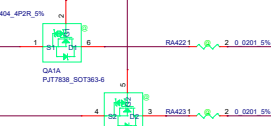
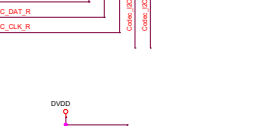
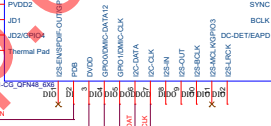
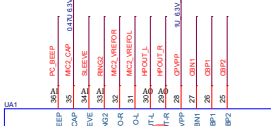
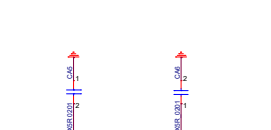
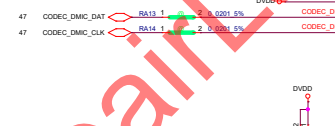
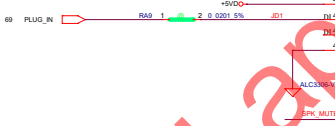
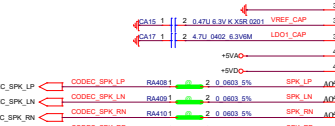
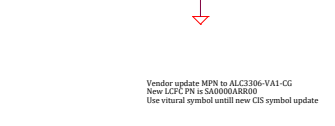
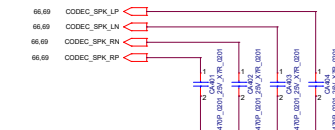
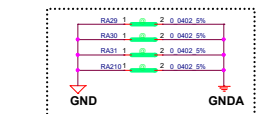
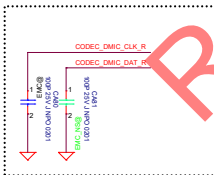
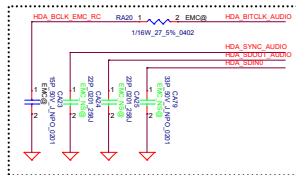
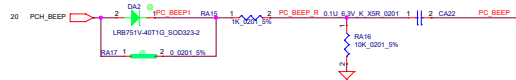
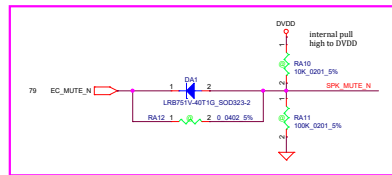


M.2 SSD(SATA/PCIE Gen3 from PCH)



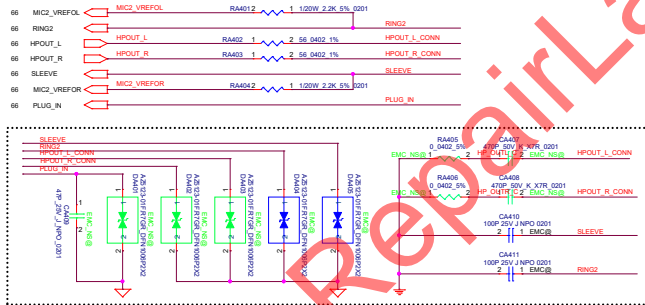
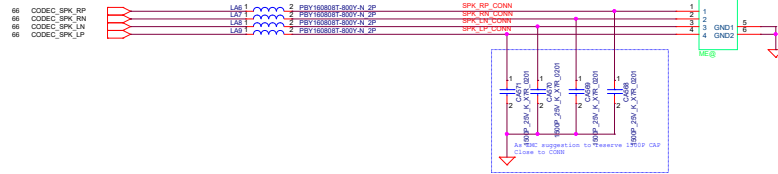


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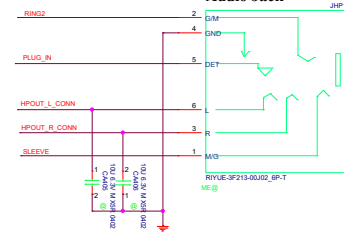


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Size	Document Number	Rev	LCFC
01	Audio Codec	0.2	
Date	Wednesday, April 07, 2021	Sheet	66 of 110

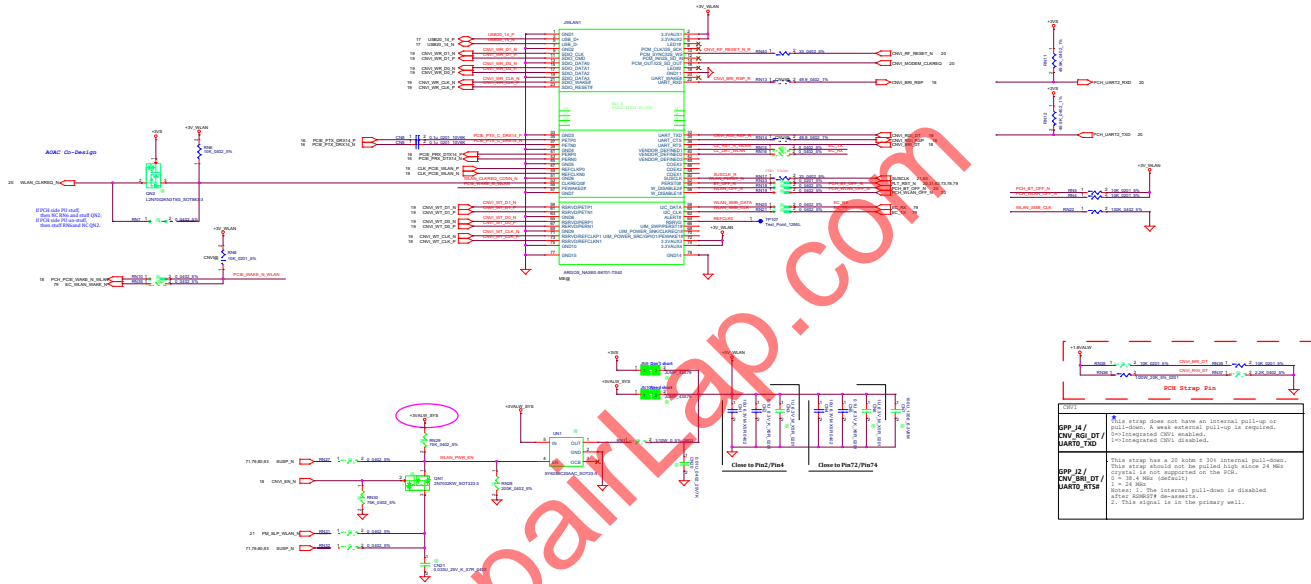
Speaker



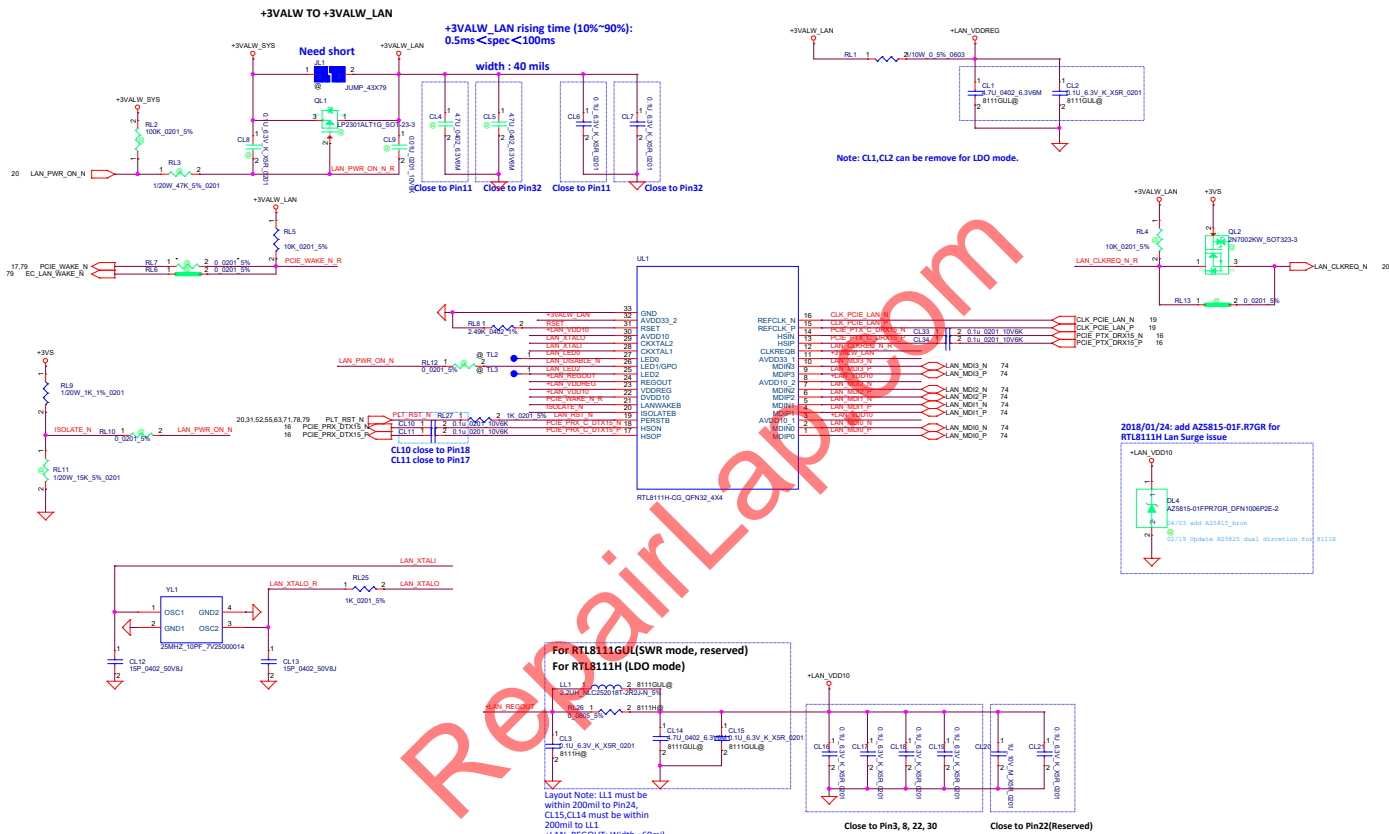
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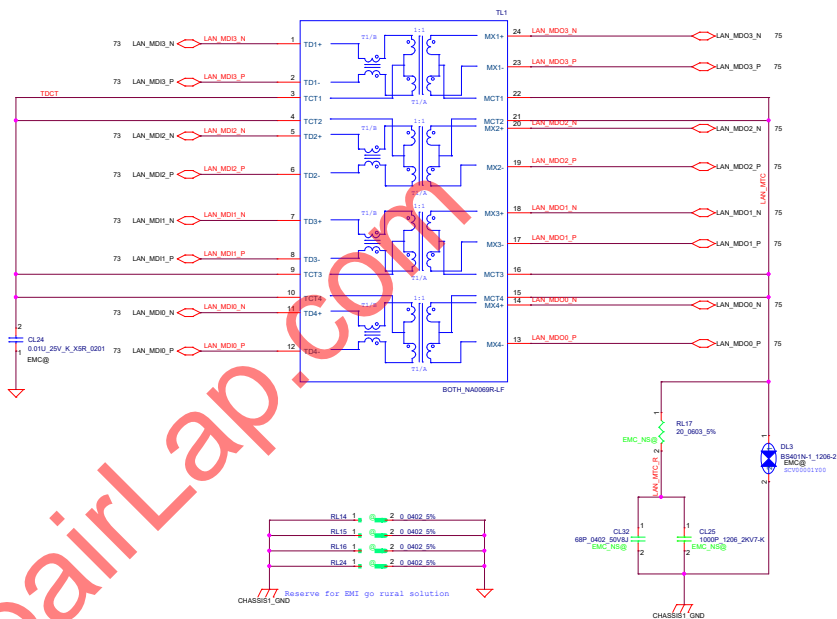
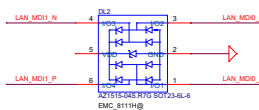
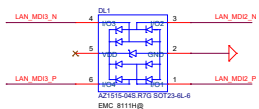
Mini-Express Card(WLAN/WiMAX)




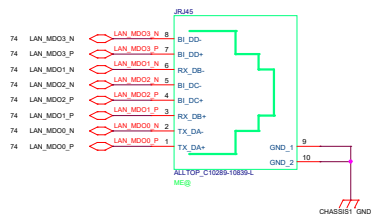
PCB Strip Pin	
<p>SPP_14 / CNV_RIS_DT / UART0_TDO</p> <p>This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=Integrated CMOS enabled. 1=Integrated CMOS disabled.</p>	<p>SPP_12 / CNV_RIS_DT / UART0_RSTB</p> <p>This strap has a 20 kOhm to 100 kOhm internal pull-down. This strap should not be pulled high since 24 MHz crystal is not supported on the PCB. 0 = 20 kOhm (default) 1 = 24 kOhm Default: 1. The internal pull-down is disabled after R806074 de-asserts. 2. This signal is on the primary well.</p>



DL1/DL2
1'S PN:SC300008P00
Place Close to TL1



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				HY 568	
Date				Wednesday, April 09, 2021	Sheet 74 of 116



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Size		Document Number				Rev		1.0	
		HW568				Date		Wednesday, April 07, 2021	
						Sheet		75 of 110	

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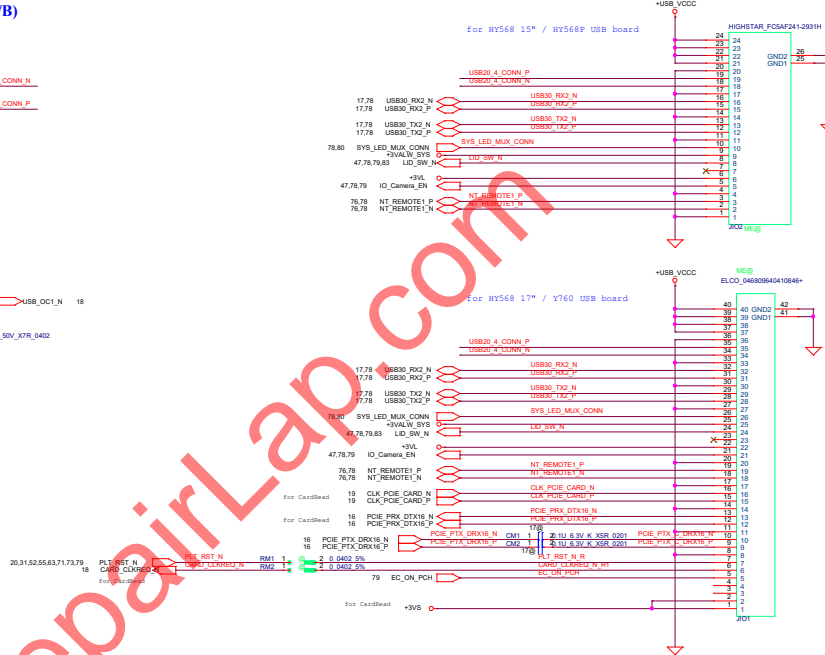
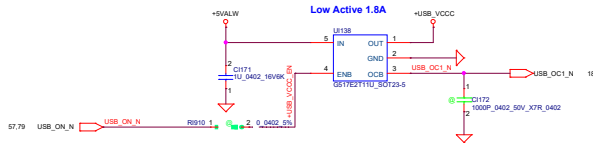
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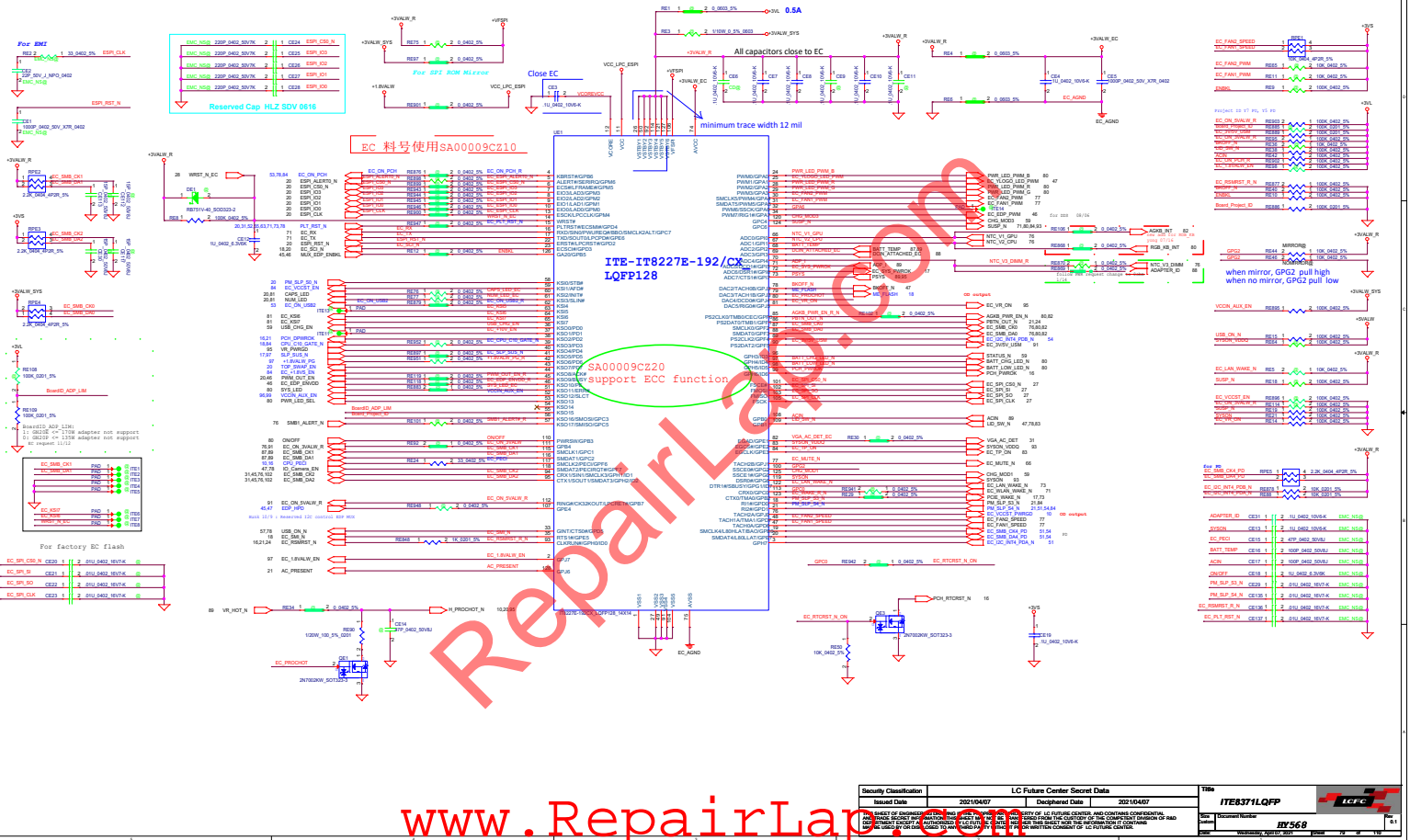
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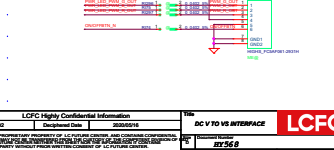
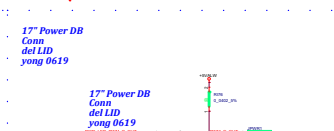
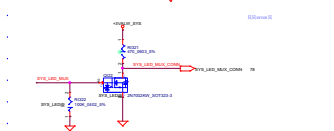
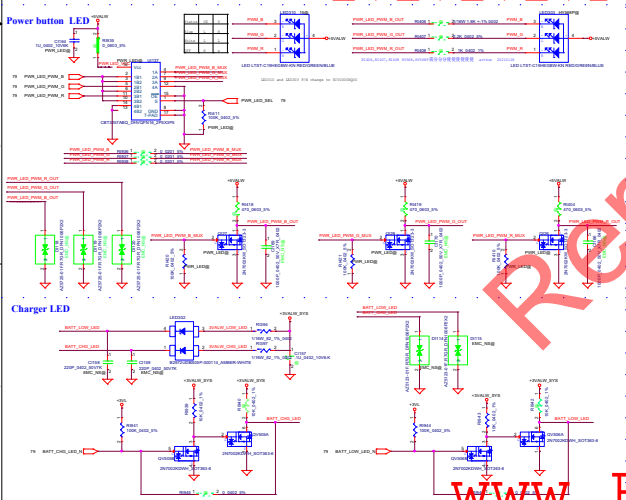
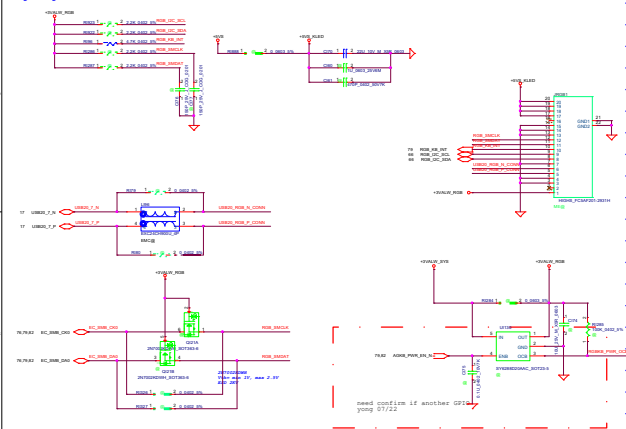


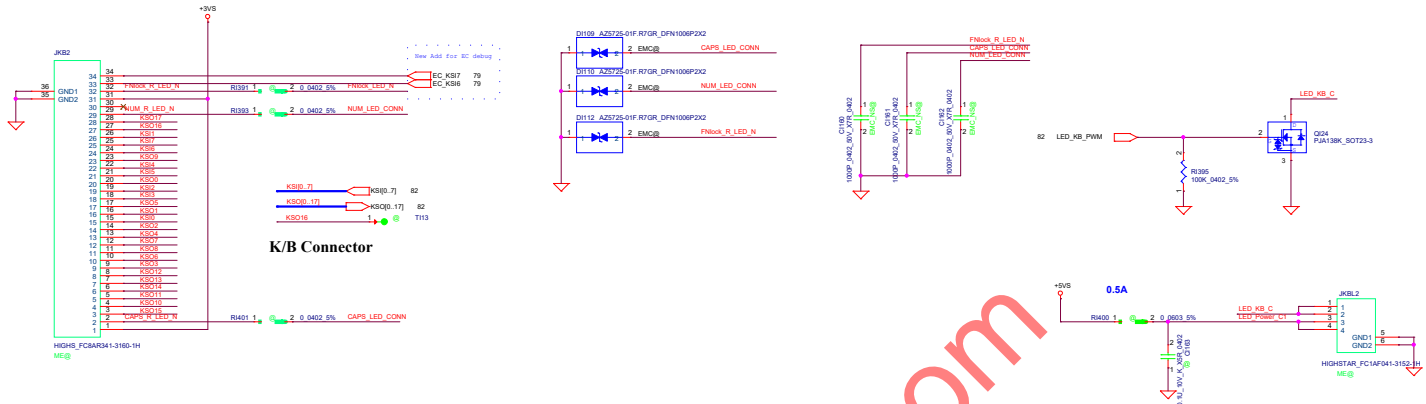
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Low Active 1.8A

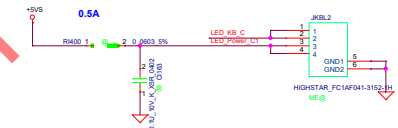
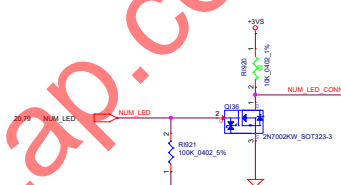
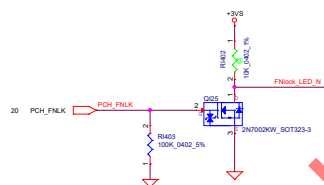
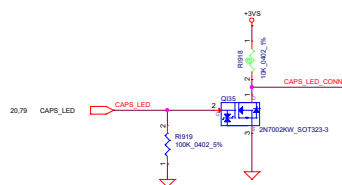
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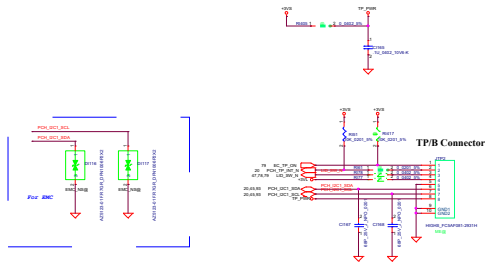
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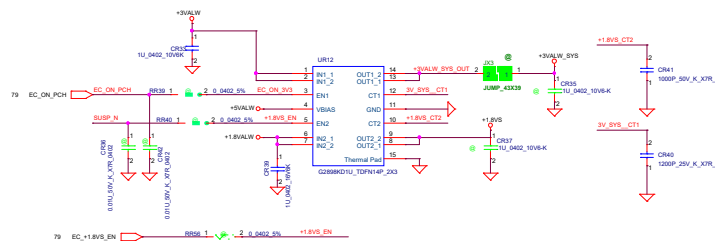
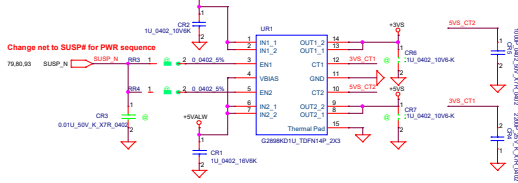
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Issued Date		Declassified Date		2020/02/24	
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[illegible]

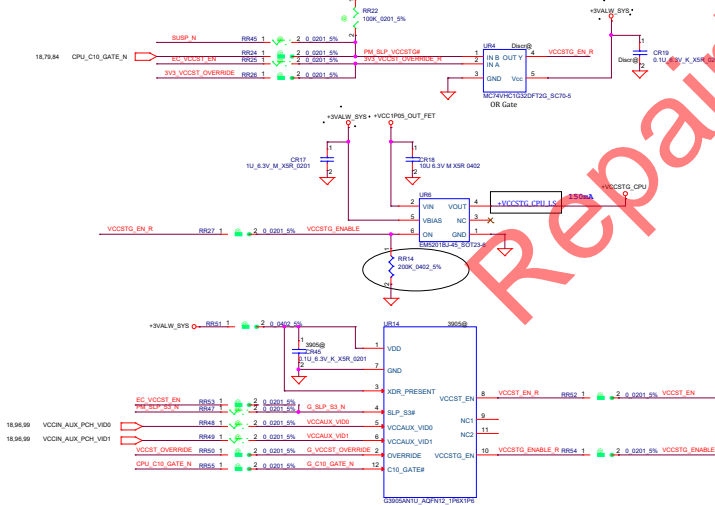
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Issued Date	20180503	Expiry/Retire Date	20200503	
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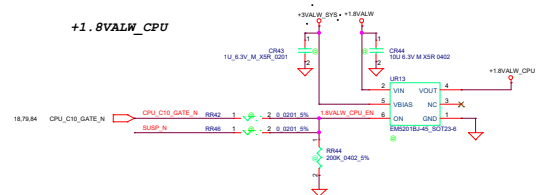
+3/SVALW to +3/VS5



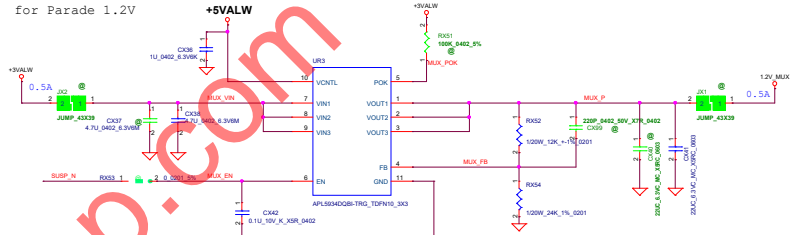
VCCSTG



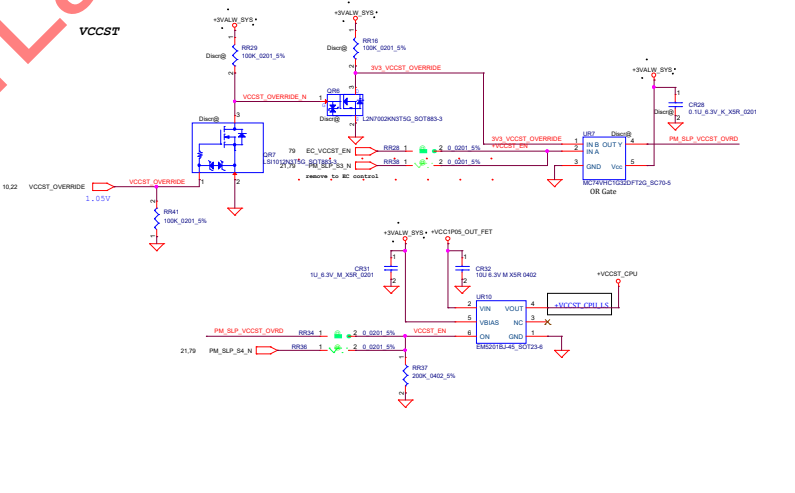
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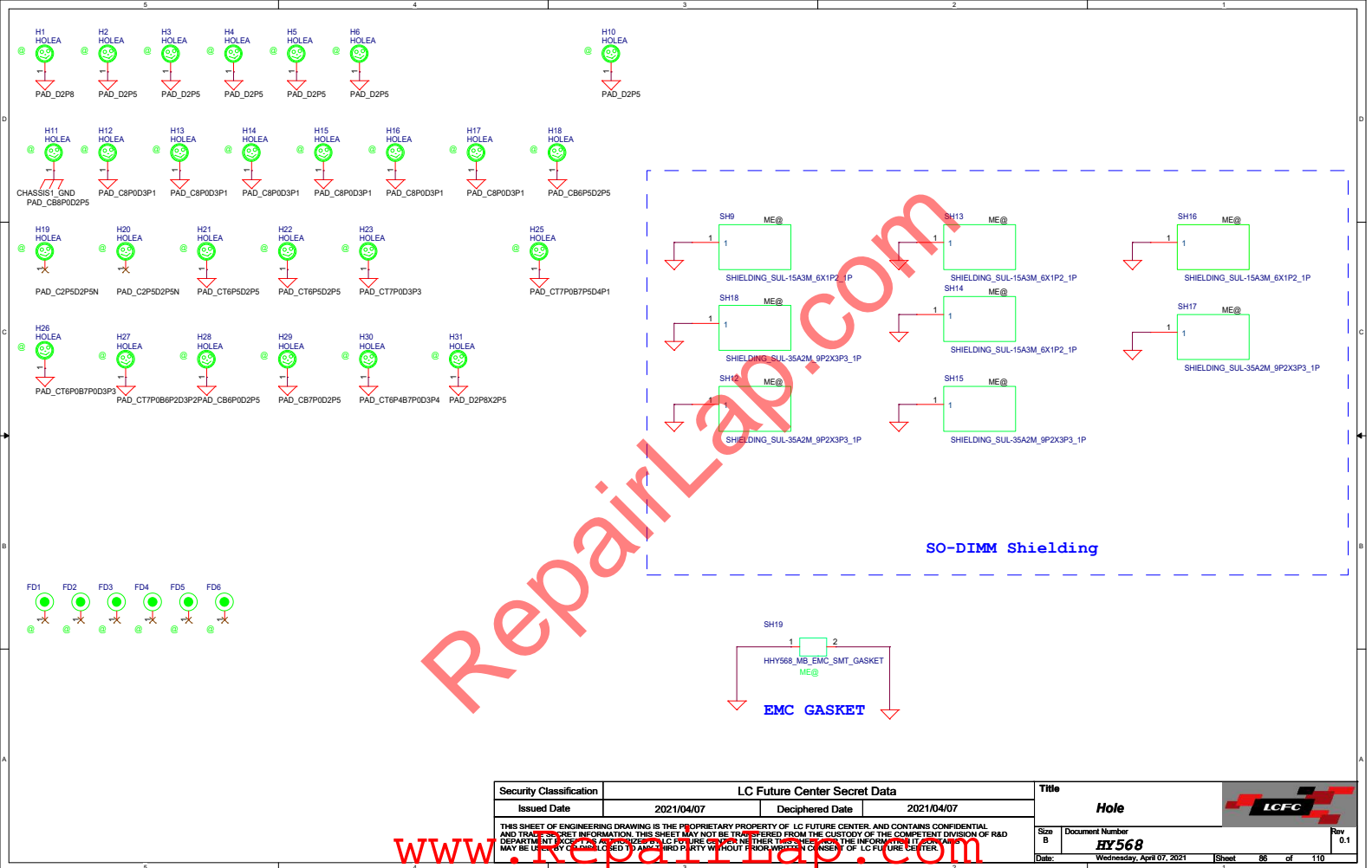


for Parade 1.2V




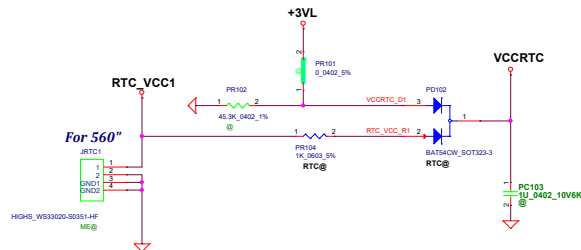
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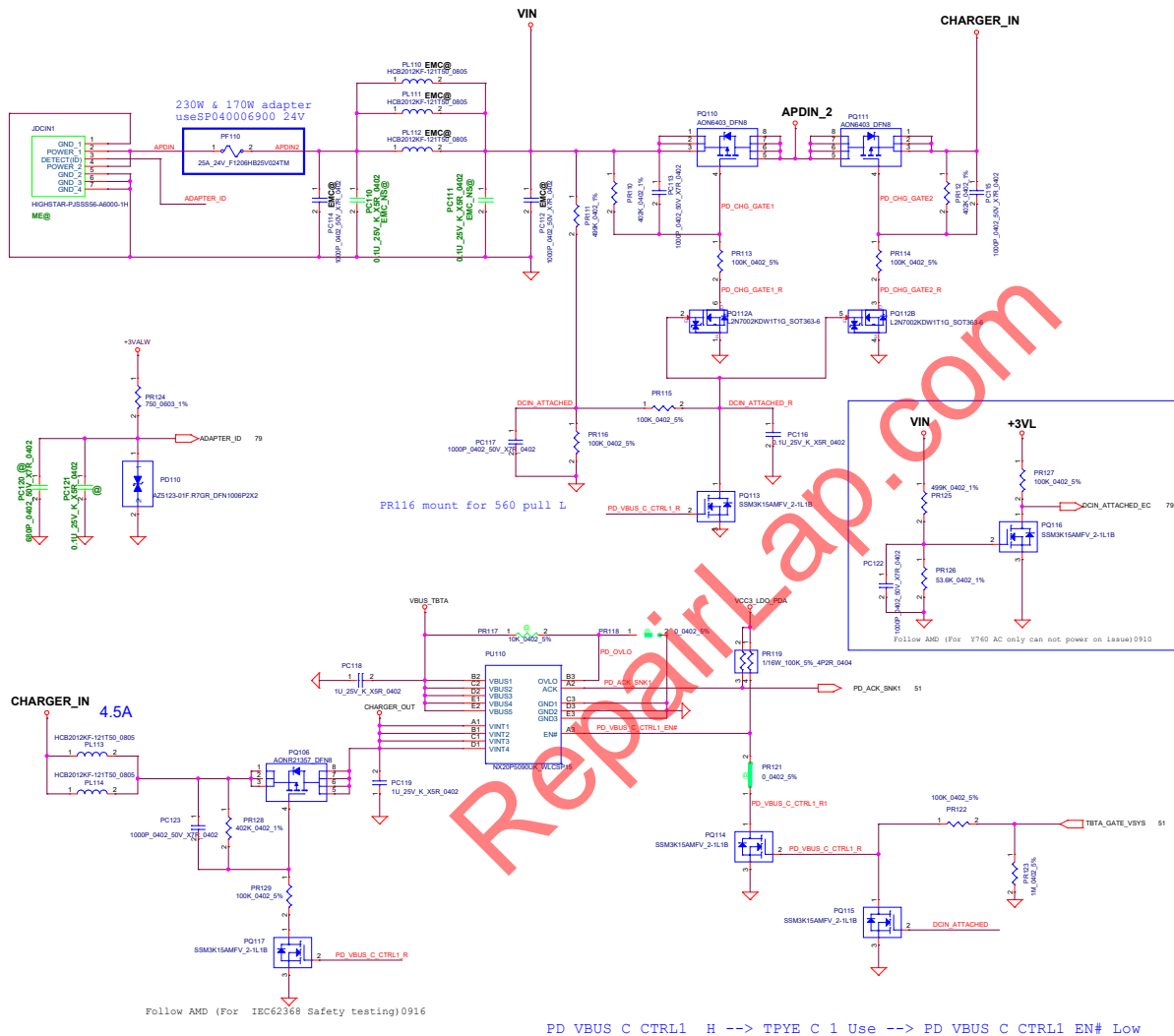




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		2021/04/07

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PWR_ACIN		BY 568 AMD	
Size	Document Number	Rev	0.1
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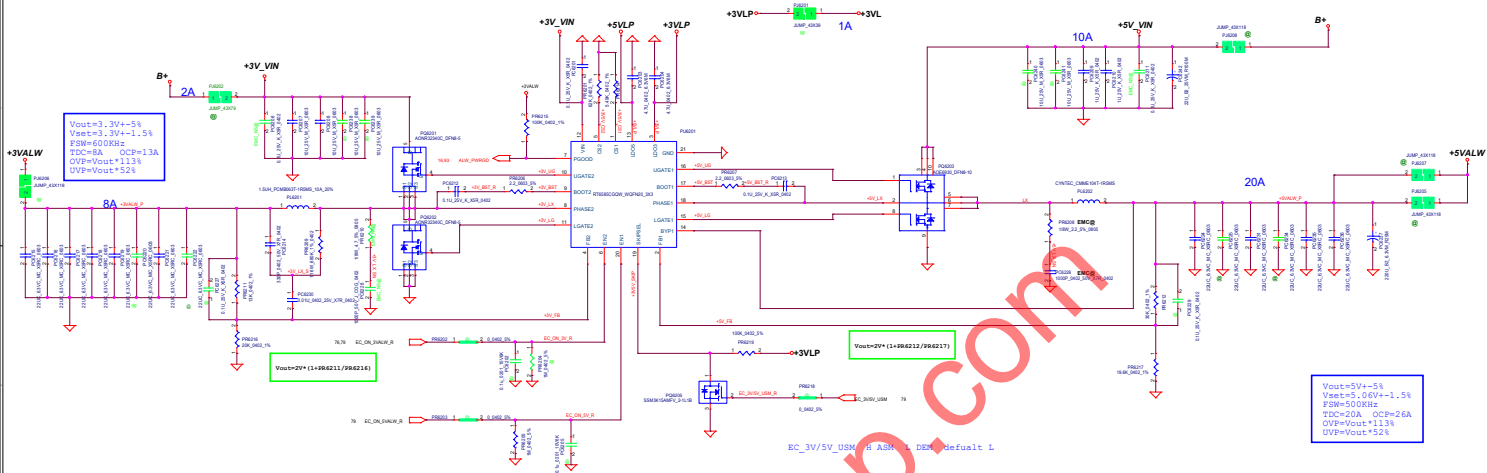
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BAT Max V=17.6V

PMON Gain=1uA/W Actuel=0.5uA/W
PR5415=15K 0.75V=100W

ICchargeLim=16.19
IDischargeLim=64.4A

V charge (MAX):17.6V
I charge (MAX):12A
FSW:800K

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				Drawn By	BY 568
				Checked By	BY 568
				Approved By	BY 568



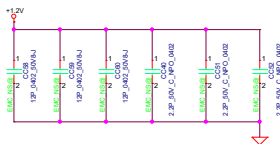
	RT6585C	RT6575D&TPS51275B
Mode	DEM/USM	USM/CCM
3V FSW	600K	355K
5V FSW	500K	300K
CSx	limit=(ilimit*Rds(on))*8/50uA	limit=(ilimit*Rds(on))*8/100uA

RT6585B&TPS51285B BOM to BOM

RT6575D&TPS51275B BOM to BOM

RT6585B&RT6575D PIN to PIN, with different work mode, FSW, and CS setting

CPU

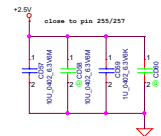


JDDR1

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM

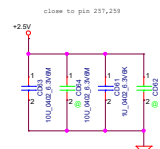



JDDRH1

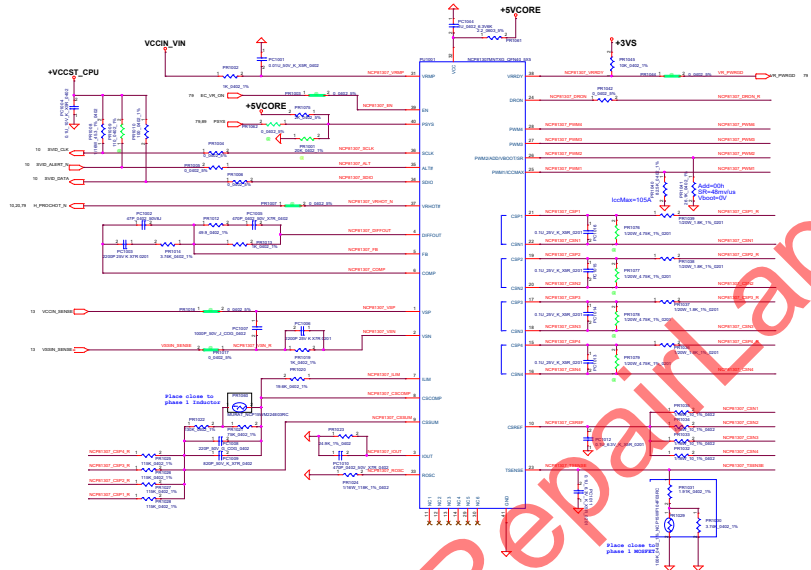
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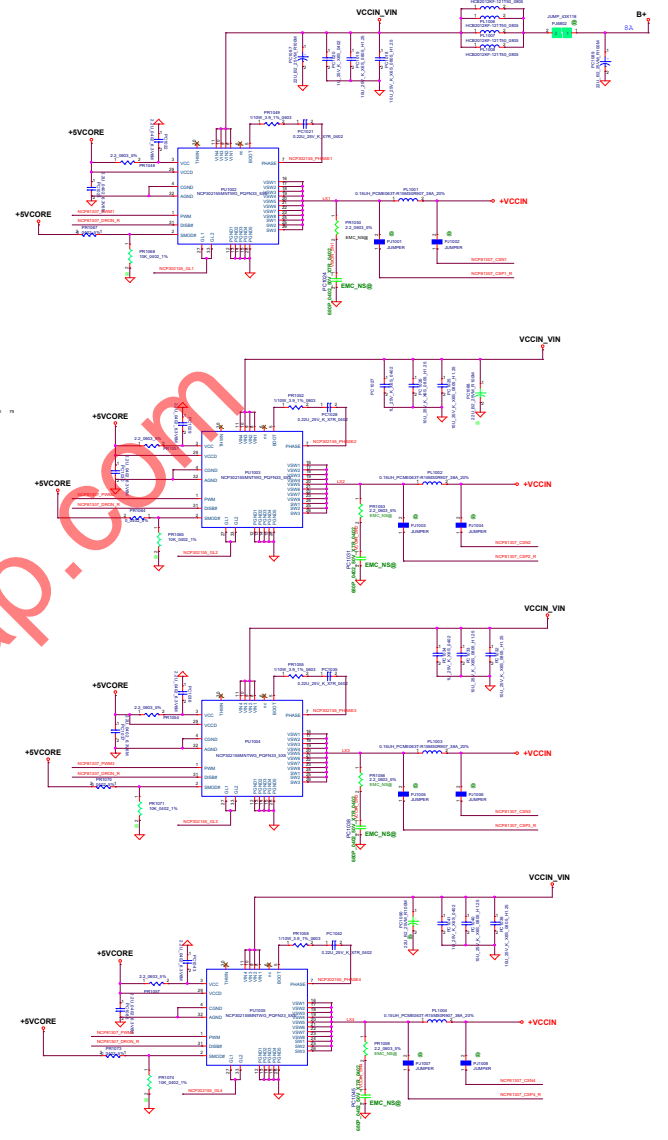
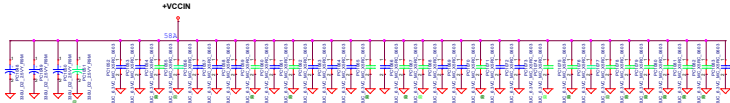
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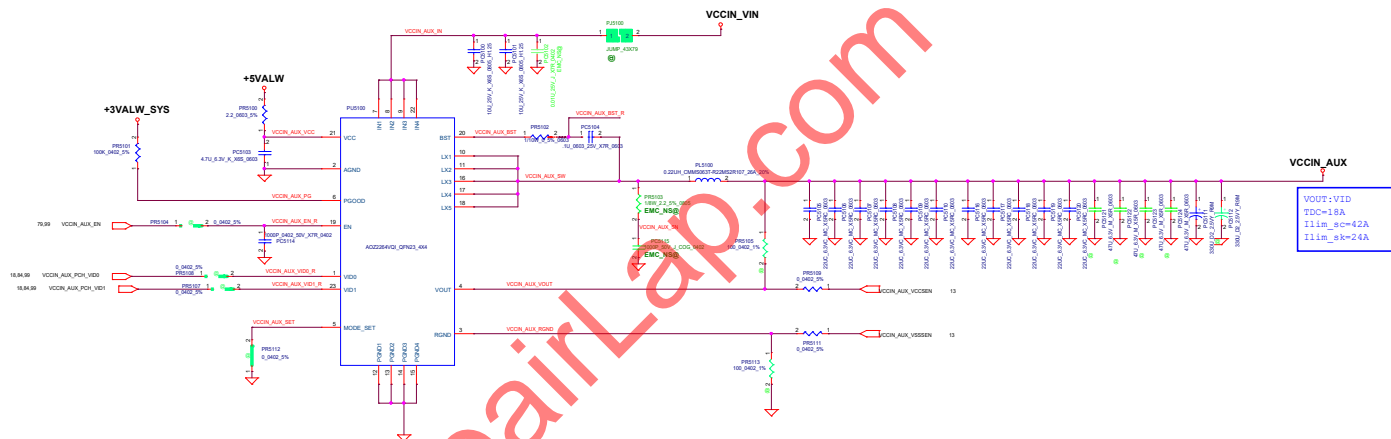
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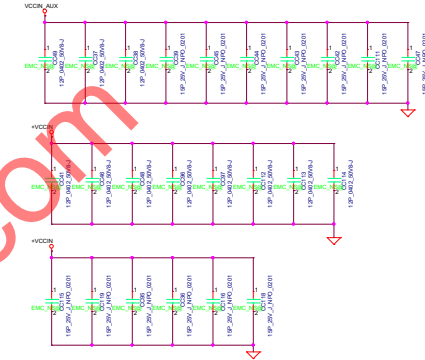
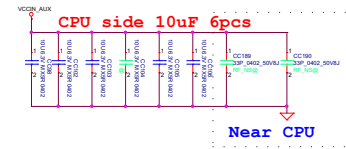
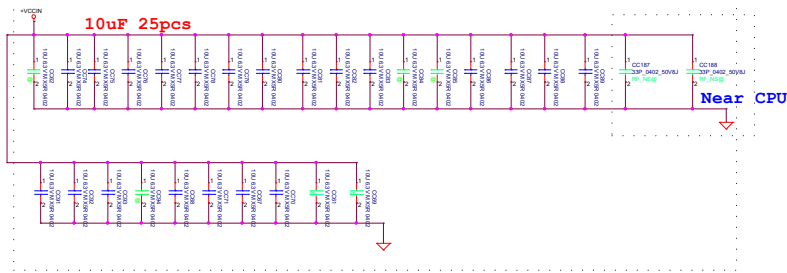


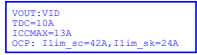
Y540: 330u*25CS*25u*15PC
 Y550: follow Y540 Vendor
 PDC: 470u*4pos*47u*13pos
 Actual: 330u*13PC*25u*15PC



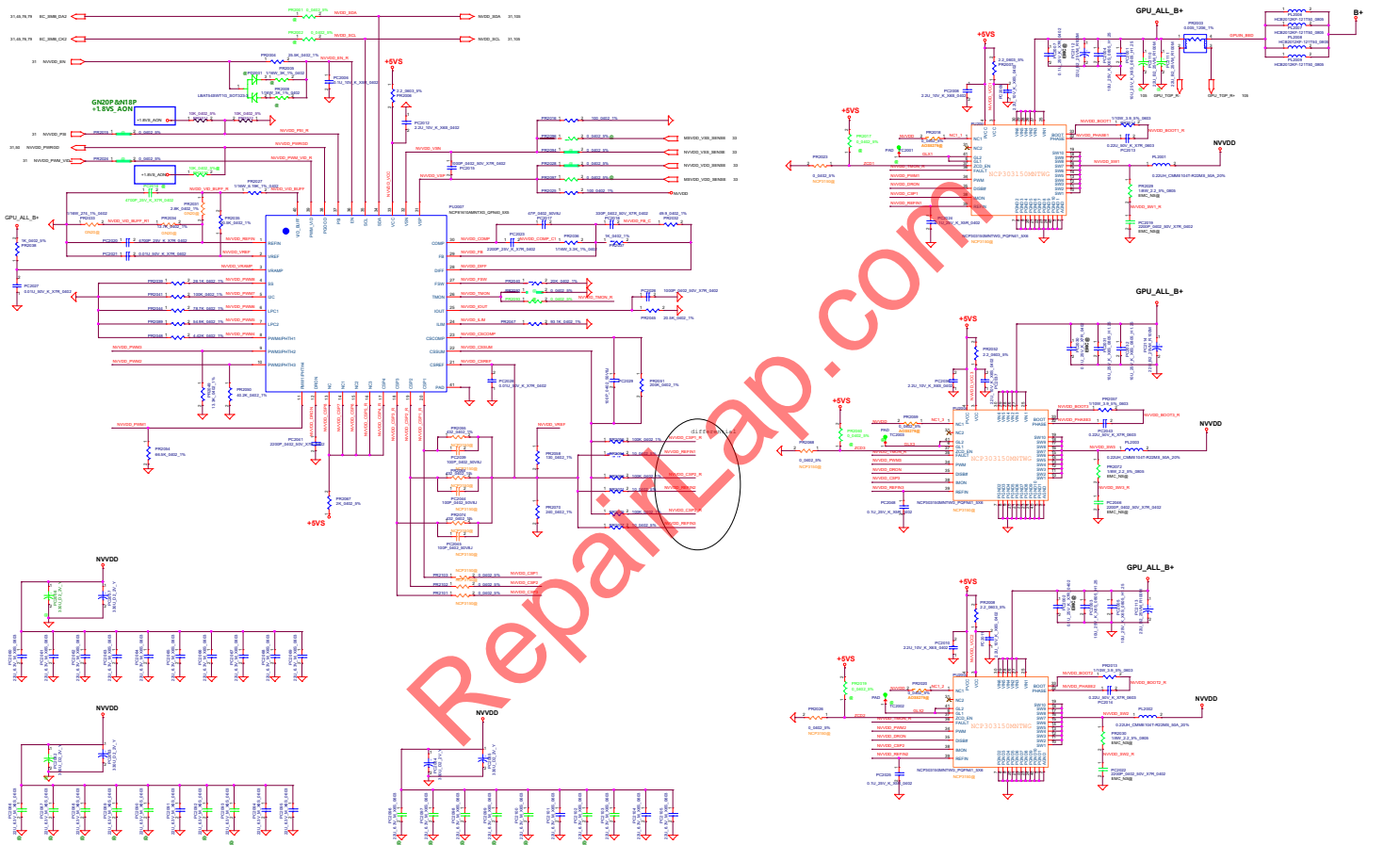
VOUT Setting	VID0	VID1
1.8V	H	H
1.65V	L	H
1.1V	H	L
0V	L	L



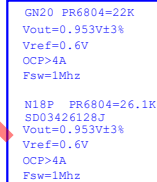




VOUT Setting	VID0	VID1
1.8V	H	H
1.65V	L	H
1.1V	H	L
0V	L	L



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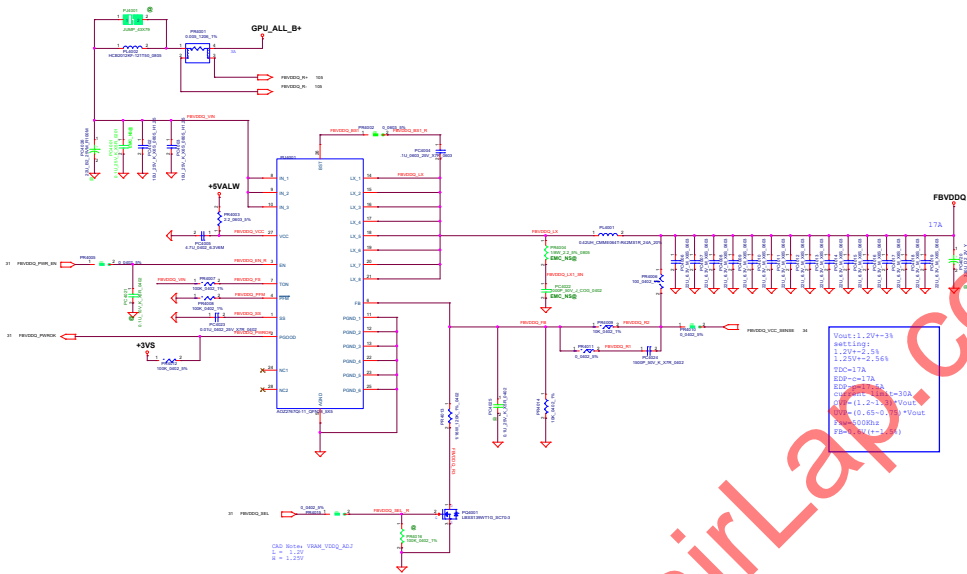
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GEN2:
BV_INX ON BV_IN2
UPI VCC
IN_NX PX ON UPI VCC
GEN1:
BV_INX ON UPI BV_IN2
IN_NX PX ON VCC
UPI GND

ADDR default is 0x6A(8 bit addr),
for 7bit addr is 0x35
a.ADDR50(pin21): 10K PU 3.3v
b.ADDR1(PIN 22): 10K PD to GND
00:0X34 01:0X35 10:0X36 11:0X37

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Doc Name	RY568 AMD			Rev	0.1
Doc Date	Wednesday, April 07, 2021	Doc Size	95	Doc	110

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